An Ultra Low-Power and Area-Efficient Baseband Processor for WBAN Transmitter

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***Abstract*—The IEEE 802.15.6-2012 standard optimized for short-range/low power purpose for WBAN applications has been approved recently. Based on the standard, this paper proposes the hardware implementation of the baseband transmitter for the first time. In our design, the physical layer (PHY) employs narrowband(NB) PHY in the standard and DPSK Modulator is optimized by employing CSD-coded (canonical signed digit) filters for low power and area-efficiency consideration. Clock gating is also implemented to cut the dynamic power in the idle state. Implemented in 130nm CMOS technology, the least total power dissipation of the transmitter is only 69.5uW at 151.8kbps and 1.0V supply in the Medical Implant Communication Service (MICS) band. In addition, The power consumption of the PHY module under different frequency bands and different data rates is investigated. The minimum energy-per-bit is only 10.1pJ/bit at 971.4kbps indicating that our PHY module is more energy-efficient than previous works.**

I. Introduction

With the development of medical technology and the increment of the elderly population, there will be tremendous growth in the healthcare monitoring markets, such as exercise monitor, health monitor for eldly people and remote patient monitoring. Patients and the aged will benefit from continuous monitoring of their diagnostic procedures. These applications can be integrated into wireless body area networks (WBANs) for health monitoring. A typical WBAN topology consists of a series of miniature invasive/non-invasive physiological sensors and is able to communicate with other nodes or with a central node [1]. Many publications have been reported about the WBAN applications for medical diagnosis, especially electrocardiography (ECG) monitoring system [2][3][4].

One of the most important issues is that the power budget is quite strict for WBAN applications because the wireless device is supplied by a battery. Due to the stringent requirements and considerations, Existing wireless communication standards such as IEEE 802.15.4 is not suitable to be used in WBAN [5]. Many investigations have been done about the low power PHY protocol for WBAN. For example, Ref. [6] proposes its own baseband PHY specification for the purposes of low complexity and low power; Ref. [7] introduces a baseband transceiver by employing an optimized PHY scheme which is compatible with IEEE 802.15.4 . Recently the IEEE Standards Association approved IEEE 802.15.6-2012 standard for WBAN applications after 5 years work of the Task Group called IEEE 802.15.6 [8]. Ref. [9] proposed the design of PHY simulator for WBAN system based on IEEE 802.15.6 by using MATLAB, but the hardware implementation has not been carried out.

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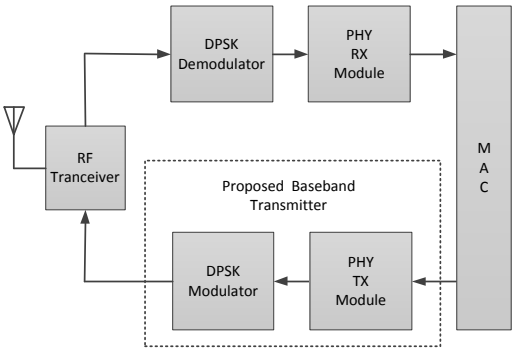

Fig. 1. Block diagram of a complete WBAN radio transceiver

As shown in Fig. 1, a low power and complexity-efficient hardware implementation of the WBAN baseband transmitter is proposed in this paper. The PHY Module is designed using the Narrowband PHY protocol in IEEE 802.15.6 standard and DPSK Modulator employs CSD-coded shaping filter for low power and area-efficiency consideration. The rest of this paper is organized as follows. Section II introduces the Narrowband PHY specification and describes the architecture of the baseband transmitter, including PHY module and DPSK modulator. CSD-based FIR filter is also discussed in this section. Section III shows the experimental results and power comparison with previous works. Finally, Section IV draws conclusions.

II. Proposed Baseband Transmitter

Three PHY layers are defined in the IEEE 802.15.6 standard, i.e., Narrowband (NB), Ultra Wideband (UWB), and Human Body Communications (HBC) layers. The selection of each PHY depends on the application requirements. This work choose the Narrowband PHY for hardware implementation. The details are introduced in the following.

A. Narrowband PHY Specification

The structure of the physical-layer protocol data unit (PPDU) packet of Narrowband PHY is illustrated in Fig. 2, which is composed of three components: the physical-layer convergence protocol (PLCP) preamble, the PLCP header, and the

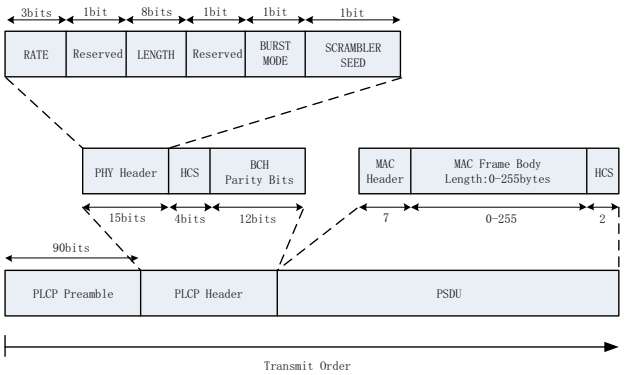

Fig. 2. IEEE 802.15.6 PPDU structure

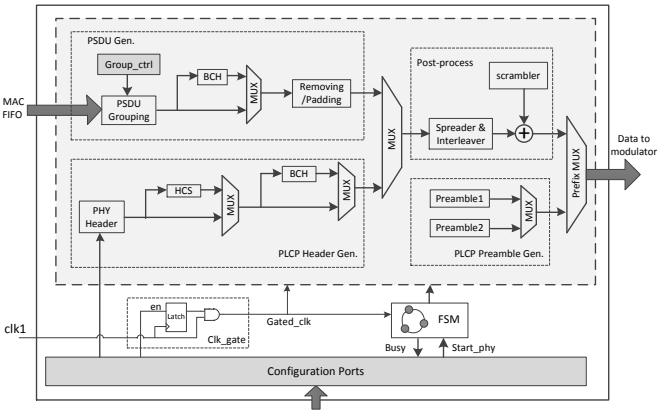

Fig. 3. Block diagram of PHY Module

physical-layer service data unit (PSDU). When transmitting the packet, the PLCP preamble is sent first, followed by the PLCP header and finally the PSDU. The reader may refer to Ref. [8] for more details.

B. PHY Module Architecture

According to the Narrowband PHY specification, this paper proposes the PHY hardware architecture of the baseband transmitter. As illustrated in Fig. 3, the PHY module is composed of five main components: PLCP Preamble generator, PLCP Header generator, PSDU generator, post-process block and finite state machine(FSM). To reduce the power consumption, clock gating is implemented to cut the dynamic power when the baseband transmitter is in idle state. The generator blocks of Preamble, Header and PSDU are responsible for generation of the corresponding components of the PPDU. Post-process block which is composed of spreader ,bit interleaver and scrambler is employed to provide robustness against error propagation and eliminate long strings of like bits that could impair receiver synchronization. All these submodules and the MUXs in the diagram are controlled by the FSM. The PHY module is interfaced with the MAC layer via MAC fifo and microcontroller (MCU) via the configuration ports. When one PSDU packet generated by the MAC layer is fed into MAC fifo and ready for transmission, the MCU will turn on the gated-clk and start FSM module by configuration ports.

As shown in Fig. 4, There are four main states in the FSM: IDLE, PREAMBLE SEND, HEADER SEND and PSDU SEND. IDLE state indicates that the PHY module does not transmit packet and all registers keep their predefined values. When there is a valid packet in the MAC fifo, the PHY module will begin to work upon receiving a start signal from MCU.

The first work state is PREAMBLE SEND state, during which the FSM will choose one 90-bit preamble sequence to transmit according to the channel number [8]. An internal counter is used to control the state transition. When the transmission of the preamble sequence is finished, i.e., counter number equals 90, the FSM will go to HEADER SEND state. In the HEADER SEND state, the PLCP Header generator block generates the PLCP Header based on the information

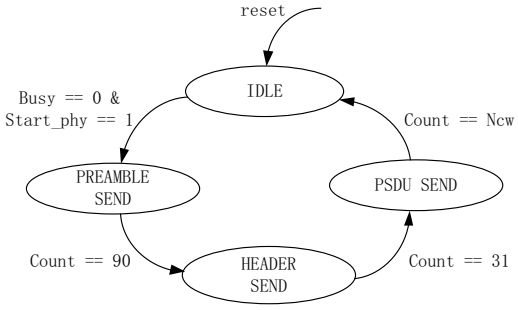

Fig. 4. PHY Module control machine

provided by the MCU and then feeds the output into post-process block for transmission. Once the 31 bits of the PLCP Header is transmitted, PHY module will go to the PSDU SEND state and PSDU generator block begin to work. As shown in Fig. 3, the messages form MAC fifo is first sent to PSDU Grouping block to divide PSDU into 51-bit segments. And shortening bits may then be appended to the messages, which are then encoded into codewords using a BCH(63, 51) encoder. The Group_ctrl block is responsible for computation of the group information which will be used to control the grouping process. After removing the shortened bits and adding pad bits, codewords will be sequently fed into post-process block. When all these codewords are transmitted (i.e., count == Ncw, Ncw is the total number of groups), PHY module will go to IDLE state and busy signal will be pulled low, which indicates that PHY module is ready for next transmission. The MCU may also turn off the gated-clk to reduce power consumption if there is no package to transmit.

C. DPSK Modulator Design

The DPSK modulator architecture is illustrated in Fig. 5, which is composed of two main components: DPSK-Mapper and the square-root raised cosine (SRRC) Pulse-shape block whose over-sampling rate is 4. Two asynchronous FIFOs are employed to pass data from DPSK-Mapper to Pulse-shape. Clock gating is also implemented to reduce the dynamic

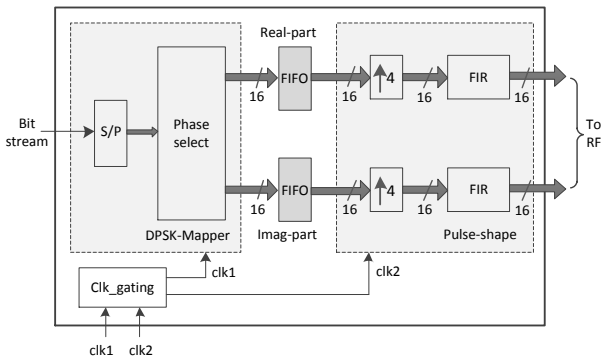

Fig. 5. Block diagram of DPSK Modulator

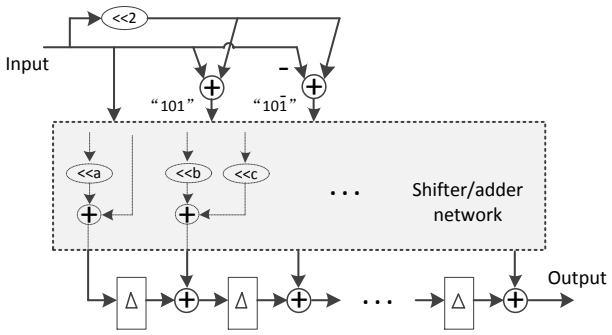

Fig. 6. CSD-based FIR filter

power consumption. Because the FIR filters in the Pulse-shape block contribute the most percent of the power dissipation, we optimize them by using multiplier-less architecture, in which the tap coefficients are represented by means of canonical signed digit (CSD) rather than binary.

The CSD number system is most popularly used over binary arithmetic in a multiple constant multiplier because of its fewer non-zero binary digits. Ref. [10] shows that the CSD-based multiplier can get 33% reduction in the number of partial product addition/subtractions. Thus the CSD technique is very suitable for FIR filters with constant coefficients.

Consider an N-tap FIR filter which can be expressed in the general form :

$$y[n] = \sum_{i=0}^{N-1} a_i \cdot x[n-i]. \tag{1}$$

If each coefficient is expressed in CSD format as $a_i = a_{iM-1}a_{iM-2}\cdots a_{i1}a_{i0}$, then the filter equation becomes :

$$y[n] = \sum_{i=0}^{N-1}\sum_{j=0}^{M-1} a_{ij} \cdot (x[n-i] << j). \tag{2}$$

where M is the word length of the coefficient, and a_{ij} assume values from a ternary set $\{0,1,\text{-}1\}$, and $<< j$ means a left shift by j bits. Thus, the computation of $y[n]$ can be visualized as summation of various shifted and delayed versions of the input x. Obviously, the number of the addition/subtraction is proportional to the number of the non-zero a_{ij}.

In addition to CSD representation, the using of common subexpressions can also give considerable hardware reduction further. Investigation of the subexpression sharing technique is carried out in [11], showing a 50% saving in the amount of hardware. It also shows that if the subexpression sharing pairs are restricted to 101 or $10\bar{1}$, one can still achieve a 33% reduction while still preserving a regular layout.

In our design, two identical 13-tap FIR filters are employed to filter the symbols and shape the spectrum. The CSD-based architecture of the filter is illustrated in Fig. 6, in which the 101 and $10\bar{1}$ pairs are selected as common subexpressions. The CSD-based FIR filter is similar with the direct form FIR filter except that multipliers are replaced by a shifter/adder network which has less redundancy. By using subexpression sharing and symmetry, the total number of adders in the network is reduced from 46 to 18.

TABLE I
COMPARISON OF DIFFERENT FIR FILTERS

FIR Type	Area(mm^2)	Power(uW)	clock(MHz)
CSD-based	0.04	31.1	1
Sequential	0.03	152.9	14
Direct Form	0.14	61.8	1

A sequential FIR filter with the same coefficients is designed for comparison purpose, which requires $order+1$ clock cycles to complete the computation. And a direct form FIR filter is also implemented. Simulation results of the three FIR filters are listed in the Table I. The power results are obtained at the same throughput rate, which means that the clock frequency of the sequential FIR filter is $order + 1$ times than the other ones. The all three filters is implemented using SMIC 130nm technology. Comparison shows that the CSD-based FIR filter is much more power-efficient than traditional architectures with a small area overhead.

III. SIMULATION AND IMPLEMENTATION

The performance of baseband PHY system is evaluated via Matlab simulations, assuming that the modulated signals

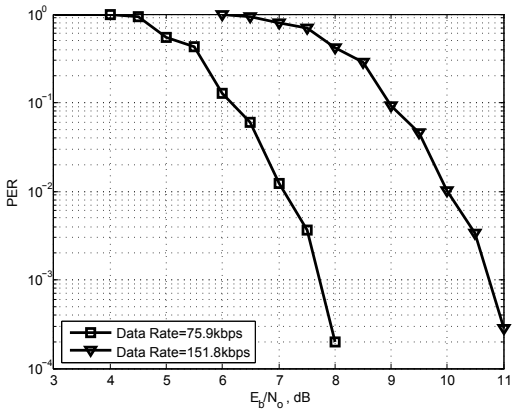

Fig. 7. Performance of baseband PHY system under MICS Band

propagate through an additive white Gaussian noise (AWGN) channel and the noise level is specified by Eb/No. The PHY system has configurable data rates (75.9-971.4kbps) and different configuration results in different robustness against noise. Fig.7 shows the simulation results of packet error rate (PER) under MICS band (402-405MHz), which indicates that low data rate should be configured in a worse communication environment to provide a more robust link.

The proposed baseband transmitter is designed in Verilog HDL and synthesized by Synopsys's Design Compiler, using the standard SMIC 0.13um technology. The core size of the transmitter is 0.13mm^2, including PHY TX module and DPSK modulator. The PrimeTime PX tool is used for power consumption analysis. Simulation results show that the least total power dissipation is only 69.5uW at 151.8kbps in the MICS band. While the maximum total power consumption is about 202uW, which is obtained at 971.4kbps in the 2360-2400MHz/2400-2483.5MHz band. Further analysis indicates that the two FIR filters in the modulator block contribute the most percent of the total power dissipation. Thus it is reasonable and essential to optimize the FIR filters by employing CSD-based architecture in section II.

To evaluate the low-power property of the IEEE 802.15.6-2012 standard, the power consumption of the PHY module is analyzed separately. The simulation results under different frequency bands and different data rates are presented in Table II. The power dissipation of the PHY module is always less than 10uW whatever the operation condition is. These results may be used as a reference, when readers design a WBAN transceiver based on the IEEE 802.15.6 standard.

The comparison between the proposed baseband PHY module and previous designs is provided in Table III. Note that in this table, the area of our design only includes PHY TX module, while the area of Ref. [4] and Ref. [7] contains PHY TX and RX modules (see Fig. 1). The minimum energy-per-bit is only 10.1pJ/bit, which is obtained at 971.4kbps. From the comparison, it can be observed that our PHY design is more energy-efficient than previous works.

TABLE II
POWER CONSUMPTION OF PHY MODULE UNDER DIFFERENT OPERATION MODES

Frequency Band (Mhz)	Modulation Type	Clock (Khz)	Data Rate (kbps)	Power (uW)
402 - 405 (MICS)	DBPSK	187.5	75.9	4.66
	DBPSK	187.5	151.8	4.60
	DQPSK	375	303.6	5.57
	D8PSK	562.5	455.4	6.55
863 - 870 902 - 928 950 - 958	DBPSK	250	101.2	5.0
	DBPSK	250	202.4	4.92
	DQPSK	500	404.8	6.22
	D8PSK	750	607.1	7.53
2360 - 2400 2400 - 2483.5	DBPSK	600	121.4	6.57
	DBPSK	600	242.9	6.9
	DBPSK	600	485.7	6.75
	DQPSK	1200	971.4	9.89

TABLE III
PERFORMANCE COMPARISON

Design	[4]	[7]			This work		
Process(nm)	180	180			130		
Power Supply(V)	1.1	1.0			1.0		
Core Area(mm^2)	0.31	1.09			0.016 [a]		
Date Rate(Mbps)	0.25	0.25	1	5	0.45	0.60	0.97
Power(uW)	34	6.1	21.0	98.0	6.55	7.53	9.89
E_b(pJ/bit)	136	24.5	21.0	19.6	14.3	12.4	10.1

[a] Note: the area of this design only includes PHY TX module, while [4] and [7] contain PHY TX and RX modules.

IV. CONCLUSION AND FUTURE WORK

This paper proposes the hardware implementation of the baseband transmitter for the WBAN applications based on IEEE 802.15.6-2012. In our design, the physical layer employs the NarrowBand PHY and the DPSK modulator is optimized by using CSD-based FIR filters to cut the power consumption. Implemented in 130nm CMOS technology, the least total power dissipation (including PHY and DPSK modulator) is only 69.5uW at 151.8kbps in the MICS band. The power consumption of the PHY module under different configuration conditions is also analyzed and comparison shows that our PHY module is more energy-efficient than previous works. To our best knowledge, the hardware of the baseband transmitter based on IEEE 802.15.6-2012 is implemented for the first time. In the future, a complete WBAN baseband transceiver will be designed and implemented soon.

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