A Fast Inter-view Mode Selection Algorithm Based on Video Array Processor

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***Abstract*— In the encoding depth map of 3D-HEVC, a fast block search algorithm is proposed to solve the problem of fixed block pattern of inter-view prediction algorithm. Variable block sizes mode is used to select prediction mode by comparing depth values, and then the algorithm is parallelly mapped to a video array processor. Compared with HTM16.2 software implementation, the average encoding time of the proposed algorithm is reduced by more than 100 times. In addition, the hardware resource usage is reduce by 27.21% with similar processing speeds.**

***Keywords*— depth map, inter-view prediction, fast search algorithm, variable block, parallel mapping**

INTRODUCTION

With the development of new video technology, 3DTV and Free Viewpoint Television (FTV), multi-view video has become increasingly popular. Multi-view Video Plus Depth (MVD) video encoding format uses 3D-HEVC texture and depth, which leads to several times amount of the data. In order to improve the compression efficiency of video encoding and encoding image quality, JCT-3V studied multi view video plus depth of MVD. Based on Multi-view Video Coding(MVC) disparity compensation prediction, 3D-HEVC introduces a series of new technologies to increase the movement parameters of inter-view prediction, disparity estimation and other related technology, the purpose is to use less relevant viewpoints and depth of information technology, enhance the encoding efficiency and reduce storage space.

The organization of this paper is as follows. In the second section, the motivation of this study is presented. In the third section, an overview of a large number of homogeneous array processor platforms are described. In the fourth section, the proposed method is described in detail. In the fifth section, experimental verification is compared and analyzed. In the sixth section, the conclusion is summarized.

MOTIVATION

Multi-view video consists of multiple views and is captured by different cameras. The inter-view prediction is a video signal obtained from different angles to capture the same scene, and it is predicted at different points of view at the same time, and there is a large amount of redundant information due to the large correlation between the various viewpoints[1].

Many researchers have proposed many fast algorithms to reduce the computational complexity of the inter-view prediction algorithms ME and DE. The reference [2] presents a fast algorithm for disparity estimation, according to the camera configuration and the macro block prediction vector of block prediction block with high accuracy using a smaller search window, low accuracy of the block using the search window for greater predictive value, thereby reducing the search range, and according to the two prediction accuracy and adaptively adjust the search area of DE and ME, to improve the encoding speed.

The [3] for the camera array parallel multi-view video camera is used for shooting, position limit the range of searching disparity estimation, and according to the prediction of motion vectors and disparity vector DV, so as to improve the encoding efficiency. In [4], iterative ME and DE algorithms are proposed to reduce the iterative search error of the inter-view prediction algorithm. In [5], a fast ME and DE algorithm is proposed to reduce the computational complexity by using the motion uniformity of the macroblock MB and the coding mode complexity. Although the proposed algorithm can save much time for multi-view video coding, it is not suitable for 3D-HEVC. In order to reduce the complexity of 3D-HEVC inter-view prediction algorithm of ME and DE, scholars have done a lot of research, mainly divided into two aspects: Fast Mode Decision (FMD) and ME/DE fast search.

In [6], an adaptive predictive search mode is proposed, which reduces the 3D-HEVC coding complexity by using the correlation between different viewpoints. The [7] proposed a view independent texture view under 3D-HEVC prediction algorithm, the algorithm analyzes the correlation between views, and designed a fast Merge mode choice and division depth selection mechanism, and the implementation of Shen[8] algorithm for fast traversal depth selection resemblance. In [9], a fast ME / DE algorithm is proposed to reduce the computational complexity of 3D-HEVC, including four fast methods, namely, early skip mode decision method, adaptive early termination mode search method, adaptive motion search range Prediction method, fast DE method. Experimental results show that the proposed algorithm can significantly reduce the computational complexity of the 3D-HEVC encoder while maintaining almost the same coding performance as full motion estimation and disparity estimation. The [10] proposed a new fast mode decision for multiview depth video encoding odd view (FMD) method, the proposed method combines the correlation between viewpoints, and analyzes the best pattern of similarity between the current encoding MB and reference MB, given the different similarity of different type of frame, design the model of decision making method different, through the statistical analysis between even and odd depth of view RD information to calculate the threshold value of RD-cost. Experimental results show that the proposed FMD algorithm can significantly reduce the complexity of MVD in depth video coding, and maintain almost the same coding quality. The improved algorithm in this paper is effective in reducing computational complexity when 3D-HEVC coding efficiency is negligible, but most of these algorithms use only spatial or temporal dependencies and do not fully study the relationship between different viewpoints the coding relevance.

In summary, there is a strong correlation between the pixels of the depth map inter-view prediction algorithm, which can be used to implement parallel execution of ME and DE operations during block matching. The video array processor proposed by the project group contains a lot of processing elements PE of the same structure, which can better meet the large-scale parallel processing of the algorithm, reduce the computing time and improve the performance of image processing applications. This paper completes the algorithm mapping in the video array processor, on the one hand has the software programmable flexible characteristic, on the other hand has the high efficiency characteristic which the hardware realizes.

□ SYSTEM OVERVIEW

This paper designs a programmable array processor to evaluate the efficiency of the proposed dynamic reconfiguration mechanism. The array structure is composed of 1024 thin-core processing elements in an adjacent interconnection, where each 4 × 4 PEs form a processing element cluster, as shown in Fig 1. The array processor consists of 32 clusters arranged in 8 by 8 structure.

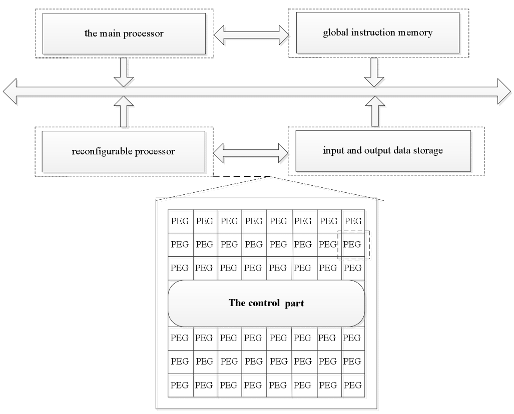

Fig. 1 Single processing element cluster

There are two kinds of data exchange methods in the cluster, which are adjacent interconnection and distributed shared storage. At the same time, it adopts hardware and software collaboration technology, so that software programmers directly manage and allocate storage resources, to achieve efficient use of on-chip storage resources. In order to meet the high bandwidth and low latency application requirements, the on-chip storage resources are segmented in the physical realization. In the local data access, the high-speed switching structure is realized, and can meet 16-channel data parallel read/write access in the 4 × 4 processing element array.

IV ALGORITHMS AND IMPLEMENTATION

A disparity estimation

There is a lot of redundant information between the various views of the inter-view prediction. In the 3D-HEVC test model, the variable size ME/DE is applied to each multi-view. Inter-view prediction is similar to the inter-frame prediction, except that the inter-frame prediction is for a single viewpoint, and the motion at the next time is predicted by the motion estimation. Analysis of various video coding standards, found to reduce the redundancy of two images widely used method is block matching, search the best match block process usually consumes a lot of computing costs. Statistics show that the inter-view prediction motion estimation between ME and disparity estimation DE has very high computational complexity, and over the entire encoder consumes more than 90% of the computation time for block matching[11]. 3D-HEVC inter-view prediction algorithm requires access to the full search in each candidate location search window, compared to find the best matching block, so the computational cost of full search is very high, the consumption of a large amount of computing time in the search process, and the algorithm complexity is O (n2). Similar to the joint model of HEVC, 3D-HEVC calculates RD-cost for all prediction modes to find a minimum RD-cost as the best prediction mode. The technique achieves high coding efficiency, but it has high computational complexity in practical applications of 3D-HEVC encoder. Therefore, without affecting the encoding efficiency, reduce the size of ME and DE to predict the 3D-HEVC variable in the process of encoding complexity, is very important for the realization of 3D-HEVC encoder, this paper calculates the depth value of the variable block mode selection, reduce the amount of computation of inter-view prediction algorithm ME/DE.

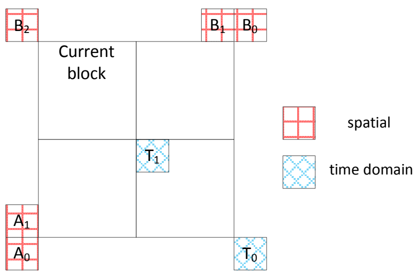

Fig. 2 parallax vector NBDV of adjacent blocks

In order to view image information using different encoding, disparity estimation is similar to the inter-view prediction of Merge motion estimation and mode of thought, in order to find the different inter-view of the matching block disparity estimation method of the current block by block adjacent disparity vector DV, obtained the disparity vector DV. In 3D-HEVC, Disparity Vector from Neighbouring Blocks (NBDV) is used to obtain the disparity vector independent encoding depth map, as shown in Fig 2. In general, for an N × N coded block, the parallax vector is obtained by the time block or the space adjacent block of the current block. The block matching order is T0, T1 and A1, B1, B0, A0, B2. The problem caused by such block matching is that the encoding time is long and the efficiency is not high. Furthermore, the choice of block size will affect the complexity of the disparity vector DV calculation, and the large block will lead to the continuity of the parallax, resulting in a larger prediction error and affect the viewpoint synthesis.

In order to select the appropriate block more accurately, realize the disparity estimation algorithm, by 3D-HEVC Test Model and the official depth map of different test sequence: Balloons, Kendo, Newapaper and PoznanStree conducted a series of experiments, analysis of the CU encoding unit depth division, the CU is mainly depth = 3 of 8 × 8 block, the proportion of the entire CU up to 65%, depth = 2 of 16 × 16 block the proportion of the second, about 26 %, Depth = 1 of the 32 × 32 block the proportion of about 7%, depth = 0 64 × 64 block the proportion of only about 2%.

Therefore, it is concluded that the distributions of different test sequences are basically the same, and the proportion of 8 × 8 blocks of depth = 3 is the largest and close to 65%, which is obviously higher than other size prediction units. With the increase of CU level, the coding time is increasing, which is due to the increase of CU depth, motion vector prediction, disparity vector prediction and syntax element export are continuously called, consuming a great deal of time. The reasonable division of the coding unit depth, select the appropriate block size of 8 × 8, to ensure the accuracy of the forecast can significantly reduce the computational complexity. At the same time, further considering the prediction unit for the size of the storage capacity requirements and, if the prediction unit adopts 8 × 8 the size of the complete disparity estimation search window pixel block size is 17 × 17 pixels, the pixel is as high as 289, and with the video in an array processor storage unit depth of 512, just can for a 8 × 8 prediction unit reference pixel block, for subsequent calculation module.

Since the difference between the two views is generally greater than the actual, for the 8 × 8 block, the parallax estimation search pixel at least 17 × 17 = 289 pixels, the complexity of the algorithm is almost 4 times the individual motion estimation. Block matching disparity estimation algorithm with data access to large amount of computation intensive, global data, media operation among independent pixel blocks, pixel processing has parallelism greatly, at the same time there are a lot of the same operating characteristics. In accordance with the order of the implementation of the algorithm, the algorithm is divided, the parallel part of the integration, thus reducing the need to solve the entire algorithm calculation time.

Multi core reconfigurable architecture has the advantages of flexibility, fast processing speed and high parallelism. It provides a platform for implementing disparity estimation algorithms. Because each PE array processors have the same structure, the configuration of the same way, support the same operations, this design can be more easily carried out mapping and scheduling algorithm, but also conducive to the realization of automatic compilation tools, with array processor with Single Instruction Multiple Data (SIMD) model of parallel computing characteristics. Therefore, combining with the analysis on a section of the algorithm of disparity estimation algorithm for block processing, different types of data blocks stored in different PE, in order to reduce the data between the calculation process and memory algorithm the number of handling, thereby optimizing the disparity estimation algorithm for computing cycle.

The specific algorithm parallel tough is: time domain adjacent blocks and airspace adjacent blocks to inspections at the same time. The time domain contiguous blocks in order for the T0, T1, select an optimal candidate, the airspace contiguous blocks in order for the A1, B1, B0, A0 and B2, selected an optimal candidate, after comparing the two choose a better, so as to find the available parallax vector, and complete a piece of disparity estimation, the current NBDV process is end. Fig. 3 is a flowchart of a parallax vector calculation. Parallelization is as follows:

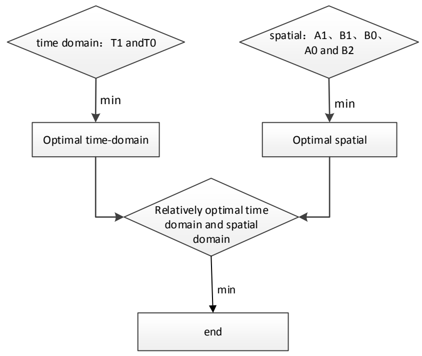

Fig. 3 Flowchart of disparity estimation

Setp1: from the current frame in accordance with the order of execution of the CTU 8 × 8 block, from the reference block to take the corresponding search window size block, the data ready to assign to a different PE;

Setp2: Simultaneously allocates the associated PEs while matching the blocks of the time domain adjacent blocks T0 and T1, the adjacent blocks A1, B1, B0, A0 and B2 of the airspace, and calculating the respective SAD values. In this process, although there is data dependency, but before the block matching data has been prepared, the impact can be almost no consideration, making different PE can operate at the same time, and calculate the respective SAD value. In this way, the operation of T0, T1, A1, B1, B0, A0 and B2 can be maximized during the block matching process. Compared with the serial implementation, the running time of the algorithm is shortened to the original 1 / 7;

Setp3: According to the SAD value calculated in the previous step, calculate the optimal SAD value of the airspace and the adjacent block of the time domain respectively, and select the minimum SAD value to get the optimal time domain and the airspace adjacent block respectively.

Setp4: according to the previous step is the minimum spatial adjacent blocks SAD value and time domain adjacent block SAD values were compared from the two SAD value in the optimal SAD, resulting in a complete disparity vector block disparity estimation.

B Inter-view mode selection

3D-HEVC encoding can be achieved at the same time reduce the redundancy among different viewpoints, this is very similar to HEVC, is different viewing position and camera number are no longer the only, while the multi view encoding, motion estimation for motion estimation and disparity estimation expansion. Inter-view prediction is mainly to the current encoding block from adjacent frames to search the best matching block, which is similar to the classic video motion estimation algorithm to find the best matching block.

Multi view video represents the same scene with similar features, so in the depth map video, the homogeneous regions predicted by viewpoints have strong spatial correlation, and the spatial neighboring blocks have similar encoding information. In the inter-view prediction in the search process, the macro block is divided into many blocks in order to capture the real video sequences accurately the real motion or disparity information, in general, the greater the division mode, the encoding complexity is smaller, more sophisticated models are classified, the greater the encoding complexity. Similar to HEVC, inter-view prediction algorithm using all possible ME/DE prediction model to perform mode decision process in 3D-HEVC, to find the minimum block matching RD-cost model, resulting in mode selection algorithm process of repeat calculation, greatly increase the computation time, at the expense of time to improve the quality of image encoding.

In order to maintain the same coding performance as the HTM prediction algorithm, a fast mode selection algorithm is proposed to solve the problem of large computational complexity in the mode selection process. By judging the different partitions from the Inter 16 × 16, Inter 16 × 8, Inter 8 × 16, Inter 8 × 8 selection, adaptively modify the block size, to achieve fast and accurate search to reduce processing time, while maintaining good image quality. In smooth image regions with a larger block to forecast, to improve the compression efficiency; and the image area change with smaller block prediction, in order to ensure the image details, the forecast accuracy, can remove redundancy effectively, reduce the encoding time, maintain the image quality.

A large number of tests were performed on the 3D-HEVC depth map, and Table 1 shows the statistical results for the different patterns of the eight test sequences. It can be seen: for the 1024 × 768 depth map test sequence, the use of Inter 16 × 16 mode, the largest number of macro blocks and the proportion of the proportion of more than 59.61%; other Inter 8 × 16 mode, Inter 16 × 8 mode And Inter 8 × 8 mode, respectively, the proportion of 8.15%, 16.69% and 15.55%. For the 1920 x 1088 test sequence, the percentage of Inter 16 × 16 mode for Depth_PoznanHall2 is as high as 73.80%, and the proportion of other Inter 8 × 16 mode, Inter 16 × 8 mode and Inter 8 × 8 mode is 6.69%, 16.67 %, 2.84%, which is related to the low complexity of the sequence pattern, the depth map has a large number of smooth areas, the movement of the object is not obvious characteristics. For Depth_PoznanStreet 1920 × 1088 test sequence, the Inter 8 × 8 mode is as high as 58.53%, and the proportion of the other Inter 16 × 16 mode, Inter 16 × 8 mode and Inter 8 × 16 mode is 16.37%, 13.03% , 12.07%, indicating that the depth of the figure in the movement of the object is relatively large.

Table. 1 Distribution of Different Patterns in Eight Test Sequences

Test	Resolving power	Inter 16×16	Inter 8×16	Inter 16×8	Inter 8×8
Depth_Balloons	1024×768	59.57%	8.08%	16.73%	15.62%
Depth_kendo	1024×768	59.70%	8.30%	16.60%	15.40%
Depth_Newspaper	1024×768	59.57%	8.08%	16.73%	15.62%
Depth_Dancer	1920×1088	25.55%	21.29%	39.53%	13.63%
Depth_Shark	1920×1088	28.96%	18.52%	23.17%	29.35%
Depth_GhostTownFly	1920×1088	2.11%	64.90%	2.5%	30.49%
Depth_PoznanHall2	1920×1088	73.80%	6.69%	16.67%	2.84%
Depth_PoznanStreet	1920×1088	16.37%	12.07%	13.03%	58.53%
Ave 1024×768	1024×768	59.61%	8.15%	16.69%	15.55%
Ave 1920×1088	1920×1088	29.36%	24.69%	18.98%	26.97%
Ave	-	40.70%	18.49%	18.12%	22.69%

In summary, of which 40.70% is determined to be Inter 16 × 16 mode, Inter 8 × 16 mode, Inter 16 × 8 mode each 18.49%, 18.12%, this is because most of the 3D-HEVC depth map is flat The area, depth change is small; Inter 8 × 8 mode is 22.69%, and the depth value near the edge of the object changes sharply. According to the above analysis, the basic idea of the inter-view mode selection algorithm is based on the depth partition, select different prediction modes, and then block the matching based on the selected mode, and adjust the various steps of mode selection between viewpoints. As shown in Figure 4, all 16 × 16 blocks are scanned first, from top to bottom, from top to bottom, and 16 × 16 blocks are divided into four 8 × 8 blocks, that is, Z0, Z1, Z2, Z3, respectively, calculate the average depth of these four blocks to determine whether the 16×16 block of the basic partition is at different depth levels, select a different model. When the mode selection is complete, block matching is performed to calculate the residual of each reference block and the current block, that is, the SAD value; and then the reference block with the smallest SAD value is selected as the most matching block for the calculation of the parallax vector. In order to obtain the best coding efficiency, all search points in the search area are redundantly searched. For each sub-block partition in the pattern, all partitions within the available patterns are iteratively executed to obtain the most efficient parallax vectors.

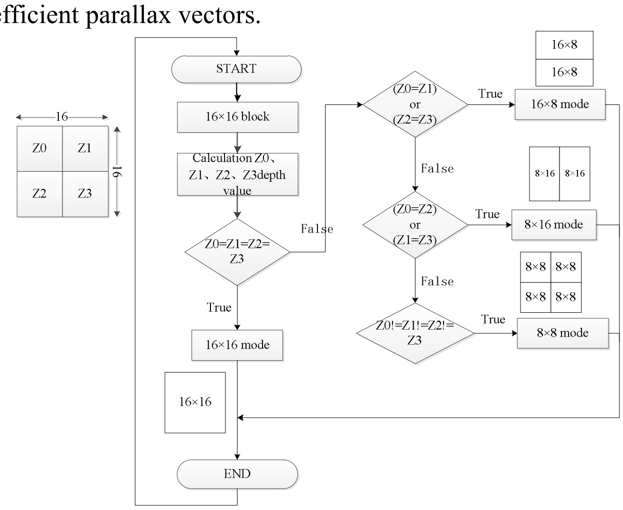

Fig. 4 Algorithm flow chart

V Results and discussion

A Intra-prediction software results

In order to verify the performance of the algorithm, after the functional simulation and FPGA testing, the performance analysis based on the mode selection of the inter-view prediction algorithm was carried out. First, we compare with the 3D-HEVC test model (HTM ver.16.2). The eight sequences published in the JCT-3V group are tested in this paper. The coding time of different test sequences is statistically analyzed under the routine test conditions of JCT-3V. In the case of three-point view (coded as: medium-left-right), the test Long frame.

The algorithm of this paper is compared with the HTM original algorithm, and the complexity of the algorithm is calculated by comparing the encoding time of the coding depth map. Table 2 and 3 are compared with the experimental results of the 3D-HEVC test model HTM16.2. It can be seen that the proposed algorithm implemented on the hardware platform video array processor can greatly reduce the coding time for all test sequences with similar coding efficiency.

Table. 2 1024 × 768 Test Sequence Coding Time Comparison

Test	HTM16.2 (time/s)	The paper(time/s)	Speed up of the proposed method
Depth_Balloons	134.083	0.7705	173.02
Depth_kendo	125.991	0.7697	162.67
Depth_Newspaper	171.571	0.7708	221.59
Ave	-	-	185.76

Table 2 is a comparison of the encoding time of the 1024 × 768 test sequences implemented on HTM and video array processors. It can be seen that compared with HTM algorithm, the time complexity of the algorithm is obvious in the array processor. For most test sequences, the proposed method can effectively save coding time compared with the 3D-HEVC encoder under the condition that the coding quality is basically the same. The results show that for the video array processor, the coding time is greatly reduced, the maximum decreases 221.59 times, the minimum decreases 162.67 times and the average decreases 185.59 times. For low motion sequences Depth_Newspaper, the encoding time is reduced is particularly high, but for the motion sequence such as Depth_Balloons and Depth_kendo rich, reduce the encoding time is still obviously.

Table 3 compares the 1920x1088 test, the HTM and the video array processor to implement the algorithm encoding time. It can be seen that the proposed algorithm can greatly reduce the coding time and reduce the average by 129.29 times when the coding efficiency of all the test sequences is negligible. For the inter-view mode selection algorithm implemented on the array processor, the encoding time of Depth_PoznanStreet test sequence is reduced by a maximum of 154.96 times; the coding time of Depth_Shark" test sequence is reduced by a minimum of 104.75 times. For a rich motion sequence such as Depth_GhostTownFly, Depth_Dancer and Depth_Poznan-Hall2, the reduction in coding time is obvious.

Table. 3 1920 × 1088 Test Sequence Coding Time Comparison

test	HTM16.2 (time/s)	The paper(time/s)	Speed up of the proposed method
Depth_Dancer	270.675	2.0077	133.82
Depth_Shark	234.777	2.2202	104.75
Depth_GhostTownFly	242.992	2.2252	108.20
Depth_PoznanHall2	274.118	1.8814	144.70
Depth_PoznanStreet	406.612	2.6072	154.96
Average	-	-	129.29

Table 4 is a comparison of the algorithms implemented in this paper with the literature **Error! Reference source not found.**, literature **Error! Reference source not found.**, and literature **Error! Reference source not found.**. The **Error! Reference source not found.** presents a fast algorithm of CACRS model, the **Error! Reference source not found.** proposed a fast mode selection algorithm for encoding depth map similarity and spatial correlation based on gray literature **Error! Reference source not found.**, proposed a fast mode ME/DE algorithm based on spatial correlation and inter-view, they are not considered in the encoding quality decrease or loss the case for model selection optimization in software. Can be seen from the table, the realization of 1.657s algorithm the average encoding time on an array processor, the proposed algorithm can greatly reduce the encoding time for all test sequences, the proposed CACRS algorithm compared with **Error! Reference source not found.**, the encoding time is greatly reduced, the average decrease of 105.63 times; compared with **Error! Reference source not found.**, reduces the encoding time on average 73.74 times; compared with **Error! Reference source not found.**, the encoding time is greatly reduced, the average decreased by 42.06 times.

Table. 4 Comparison of 8 Test Sequence Coding Time

test	HTM16.2 (time/s)	Error! Reference source not found. (time/s)	Error! Reference source not found. (time/s)	Error! Reference source not found. (time/s)	The paper (time/s)
Depth_Balloons	134.083	92.115	76.526	47.063	0.7705
Depth_kendo	125.991	97.975	77.231	59.574	0.7697
Depth_Newspaper	171.571	129.365	98.435	55.436	0.7708
Depth_Dancer	270.675	215.699	124.984	60.317	2.0077
Depth_Shark	234.777	184.382	146.745	59.807	2.2202
Depth_GhostTownFly	242.992	199.037	115.604	54.255	2.2252
Depth_PoznanHall2	274.118	211.052	142.982	95.264	1.8814
Depth_PoznanStreet	406.61	283.815	208.259	139.061	2.6072
Ave 1024×768	143.882	106.485	84.064	54.024	0.7703

Ave 1920×1088	285.834	218.797	147.715	81.741	2.1883
Ave	232.602	176.680	123.846	71.347	1.657

The proposed algorithm is implemented on a video array processor, with a much lower coding time and an average coding time of 150.46 times. Analysis shows that the algorithm designed in this paper can reduce the coding time quicker, which has more advantages than the software implementation, and the average encoding time is reduced more than 100 times.

B Dedicated hardware results

In order to facilitate the comparison of the operating period with the algorithm implemented in [12], the advantage of the parallax estimation algorithm implemented in this paper is discussed in this paper. The Virtex-7 XC7VX485T chip used in ISE of [12], as shown in Table 5. In the T-AWDE array structure, the parallax estimation algorithm is implemented. The integrated frequency is 175MHz. During the parallax estimation process, 49 processors are used to calculate 49 pixels in 198 clock cycles. Each pixel processing time is 2.1 × 10-8s. The parallax estimate designed in this paper is based on the video array processor proposed by the project team. The integrated frequency is 125MHz. Using 12 processors to complete 64 pixels using 850 cycles, each pixel processing time is 1.06 × 10-7s. In order to better speed up the processing time of each pixel, the number of processors is increased when the parallax estimation algorithm is implemented. When the number of processors is increased to 60, the algorithm designed in this paper is an average of the processing time is 2.11 × 10-8s.

Table. 5 Comparison of run times

	FPGA	**Processing kernel number**	**Each pixel time /s**	**frequency/MHz**	**LUTs**
[12]	Virtex-7 XC7VX485T	49	2.1×10^{-8}	175	152k
The paper	Virtex-7 XC7VX485T	12	10.6×10^{-8}	125	23k
		48	3.54×10^{-8}		90k
		60	2.11×10^{-8}		112k
performance analysis	-	-	+0.48%	-	-27.21%

It can be concluded that the parallax estimation algorithm implemented in the array processor is lower than that in **Error! Reference source not found.**. When the number of processor cores is 60, the speed of this paper is higher than that of **Error! Reference source not found.** to slow 10-10s, slow 0.48%, but basically consistent. In terms of resource occupancy, it is less than the processor LUTs designed in **Error! Reference source not found.**, using less than 40k, down by 27.21%.

VI CONCLUSIONS

According to the software implementation of disparity estimation algorithm with large amount of data, the speed is slow, the video processor array based on parallel implementation scheme is proposed for disparity estimation, inter-view prediction model of the partitioning algorithm, the encoding complexity is smaller, more fine pattern classification problem, the encoding complexity is larger, statistical analysis different test sequence distribution mode selection, by comparing the depth values, adaptive selection of block mode selection algorithm can realize parallel mapping model between 3D-HEVC depth map view. In the premise of ensuring encoding quality, compared with the HTM16.2 encoding time for 1024 × 768 and 1920 × 1088 test sequences, the proposed algorithm in video array processor, the encoding time is greatly reduced, reducing the average 138.78 times.

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