A Buck-Boost Hybrid DC-DC Converter for Wearable Health Monitoring Devices

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***Abstract*—A hybrid approach of the DC-DC conversion is presented for battery-operated portable electronics systems such as wearable health monitoring devices. A switched-capacitor (SC) DC-DC converter is steered by hysteretic control to provide buck-boost conversion with a flexible conversion ratio, and its output is regulated by a low-drop-out (LDO) regulator delivering a low-ripple DC output. The SC DC-DC converter consists of only 4 switches and 2 capacitors, and employs a combination of NMOS and PMOS transistors simplifying the gate drive scheme. The converter has been designed to work up to 30MHz switching frequency and provides 2.8V output from a battery supply varying from 3.5 to 2V over its discharge cycle. It has been fabricated in 0.18μm CMOS technology.**

I. INTRODUCTION

In portable battery-operated applications, the power management has become one of the most important functions, since it can significantly increase the battery life by providing the optimal supply voltage to the circuitry despite the varying battery voltage over its discharge cycle. Especially in wireless health monitoring devices, the battery life is directly linked to the device cost and user convenience [1]. The power management in battery-operated systems incorporates a DC-DC converter to generate a regulated output voltage. The DC-DC converters can be classified into three categories – inductor-based converters, linear regulators and SC-based converters. Inductor-based DC-DC converters are commonly used for medium- to high-power applications and they are flexible in providing different levels of a regulated output voltage which may be higher or lower than the input voltage. However, such converters are not suitable for the integration due to the use of inductors or transformers. On the other hand, linear regulators can be easily integrated on chip. However, a linear regulator can only provide an output voltage lower than the input voltage. A SC-based DC-DC conversion is employed usually for low-power applications. The SC architecture uses switches and capacitors to convert voltages and is therefore suited for monolithic integration.

The SC DC-DC converters, however, result in higher output ripple as compared to the other types of converters. Moreover, their use is limited since only the fixed voltage conversion ratios can be implemented. If the input voltage changes, the converter has to be re-designed to adjust the conversion ratio. To overcome this, a configurable SC DC-DC converter is proposed [2], which changes its topology based on the input voltage by using 9 switches and 2 capacitors to adjust the step-down voltage ratio. Similarly, a reconfigurable architecture is proposed for stepping the voltage up [3], and it requires 18 switches and 4 capacitors. On the other hand, two different switched-capacitor converters can be used [4] to obtain two different output voltages, one of which is higher and the other is lower than the input voltage. A multiple-voltage-gain SC DC-DC converter has been proposed [5]. It requires 20 switches and 3 capacitors to configure the gain.

In this paper, a buck-boost hybrid DC-DC converter designed for watch-type wireless blood pressure monitoring devices is presented. The device operates with a single-cell Lithium battery providing a nominal voltage output of 3V. However, the voltage could reach up to 3.5V at the beginning of discharging and down to 2V near the end of its life. A 4-switch 2-capacitor SC DC-DC converter is designed to operate in buck-boost mode and followed by an LDO regulator to provide well-regulated low-ripple DC output. A simple voltage-mode hysteretic controller is used together with a combination of NMOS and PMOS switches for reducing circuit complexity without compromising performance. The presented design is well suited for integration.

II. CONVERTER ARCHITECHTURE

The converter architecture is shown in Fig. 1(a). A low-ripple buck-boost DC-DC converter is realized by employing both the SC converter and the LDO regulator. The SC converter generates V_{bus} of 3V regardless of the battery voltage varying in the range of 2 to 3.5V and the following LDO regulator finally delivers well-regulated 2.8V DC supply to the rest of circuitry.

A. Switched-Capacitor DC-DC Converter

The circuit schematic of the SC converter is shown in Fig. 1(b). It comprises of 4 switches, a flying capacitor C_1 and an output capacitor C_2. Its operation can be divided into two phases:

In the charging phase Φ_1, the switches S_2 and S_4 are turned on (S_1 and S_3 are off) and the flying capacitor C_1 is charged to V_{bat}. During this phase, the output capacitor C_2 continues to supply the load current and is being discharged.

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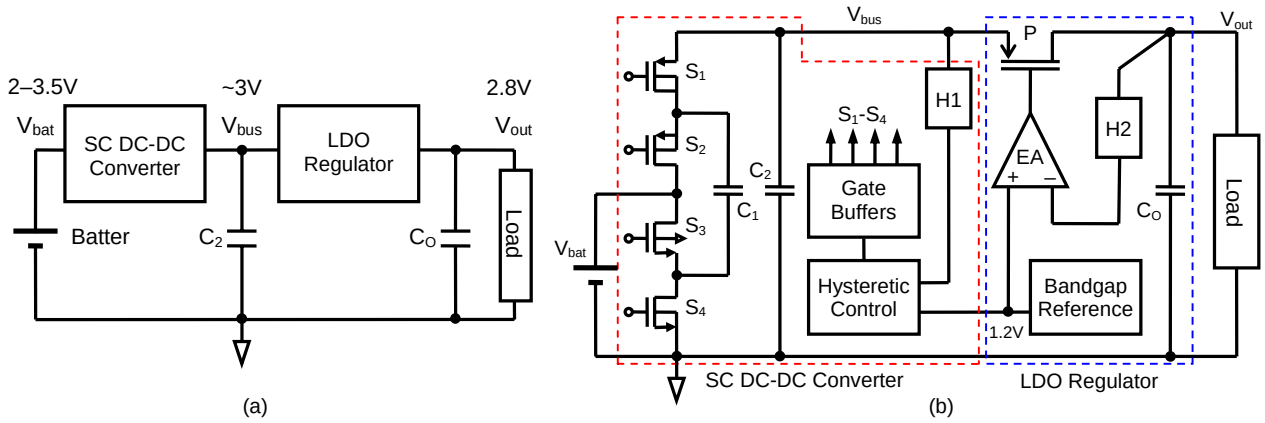

Figure 1. (a) Architecture and (b) functional block digram of the buck-boost hybrid DC-DC converser

In the transfer phase Φ_2, S_1 and S_3 are turned on (S_2 and S_4 are off). C_1 which was charged to V_{bat} in Φ_1 is now in series with the input source. These two voltage sources charge up C_2. Thus by controlling the frequency and duration of transfer phase operation, the voltage on C_2 (bus voltage V_{bus}) can be controlled.

The charge and transfer phase pulses normally have a duty cycle of 50%. To transfer the energy from input to output, these phases are periodically repeated. For this operation, a small hysteresis band is chosen around the reference voltage, as shown in Fig 2. We denote the upper threshold as V_{ref+} and the lower threshold as V_{ref-}. When the output voltage falls below V_{ref-}, the pulses are repeated alternating Φ_1 and Φ_2, which charges the output capacitor. Once the output voltage exceeds V_{ref+}, the pulses are blocked and no energy transfer takes place. The flying capacitor is kept charged up for the next cycle. In this mode, the output capacitor continues to provide the load current, which causes the output voltage to drop. The cycle is repeated, once the voltage falls below the V_{ref-}. Doing so, the output voltage is regulated around the required level V_{ref}, but it introduces a ripple due to the nature of the controller operation. In order to filter out the voltage ripple resulting from the hysteretic voltage control, a LDO regulator is used as a post regulator.

B. Low-Drop-Out Regulator

Linear regulators are broadly used for low-ripple DC-DC conversion [6]. Most linear regulators use a PMOS as a pass transistor (P) which is controlled by an error amplifier (EA) with negative feedback that monitors the output voltage and compares it to the reference voltage. The output of EA controls the gate voltage of the transistor P. The simplified schematic of an LDO is shown in Fig. 1(b). The PMOS should stay in saturation regime for the proper regulation operation. Due to closed-loop operation, EA adjusts the gate voltage of P so as to minimize the voltage error at its input terminals. In other words, the EA adjusts the voltage drop across the transistor, so as to maintain the output voltage at the desired value.

Therefore the output of the LDO can only be lower than the supply voltage and a drop-out voltage of around 200mV is usually chosen. For 2.8V output, the SC DC-DC provides an output of 3V which is further regulated to the desired level.

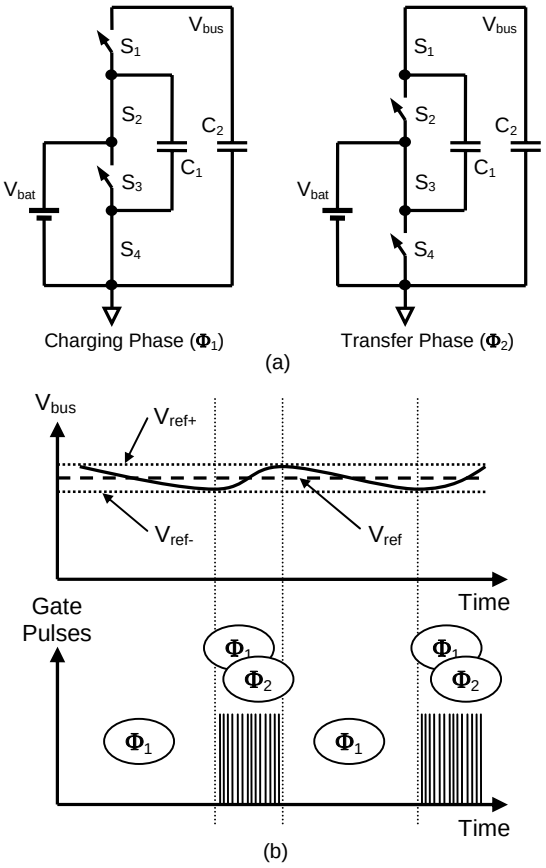

Figure 2. Hysteretic control of SC DC-DC converter

C. *Gate Drive Requirements*

Gate drivers are required in most switching power converters to provide on/off control of both ground-referenced and floating switches. If NMOS transistors are used to realize all the switches, level shifters are required to turn on/off these switches [3],[4]. In order to eliminate this requirement, a combination of PMOS and NMOS transistors is used to realize the switches. The upper two switches (S_1 and S_2) are realized using PMOS transistors, while the lower two switches (S_3 and S_4) are realized using NMOS transistors. Appropriate substrate connections are required so as to avoid the forward-biasing of source/drain-to-body junctions. The shoot-through is eliminated by using non-overlap clock signals, which is passed through a series of buffers for increasing the fan-out of the gate signals.

III. EXPERIMENTAL RESULTS

The chip was fabricated in a 0.18µm CMOS process. Fig. 3 shows the die micrograph of the test chip which measures 1578µm × 1578µm. The SC-DC-DC converter has an active area of 437µm × 310µm. 5 LDOs were integrated into the same die, occupying an active area of 933µm × 468µm.

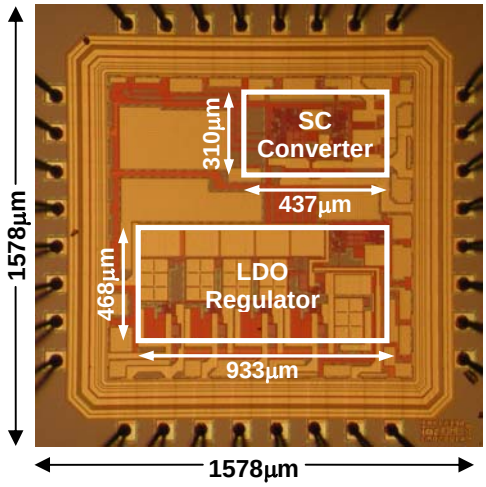

Figure 3. Die micrograph of the buck-boost hybrid DC-DC converter

The overall performance relies on the quality of the bus voltage. This test chip allows testing the LDO regulators and SC DC-DC converter independently. The clock frequency to the SC DC-DC converter was set at 5MHz. The start-up response is shown in Fig. 4. It takes 36µs to start up when the input voltage is 3.3V. When the input voltage is reduced to 2.6V, the SC DC-DC converter takes 112µs for start-up.

The output of the SC DC-DC converter is maintained at 3V despite the variations in input voltage as shown in Fig. 5. When the output of the DC-DC converter V_{bus} is connected to the LDO input, the output voltage as a function of the input voltage is shown in Fig. 5. A variation of less than 20mV is observed in the LDO output voltage over the input voltage range of 2 to 3.5V when the switching frequency is 5MHz.

The SC DC-DC converter is tested with varying the switching frequency. V_{bus} is shown as a function of switching frequency in Fig. 6. Curves are drawn for two different voltages – one when the converter is operating in step-up mode (with V_{bat}=2.6V) and the other when it is operating in step-down mode (with V_{bat}=3.5V). It is seen that for switching frequencies higher than 7MHz, the bus voltage is nearly independent of switching frequency and input voltage.

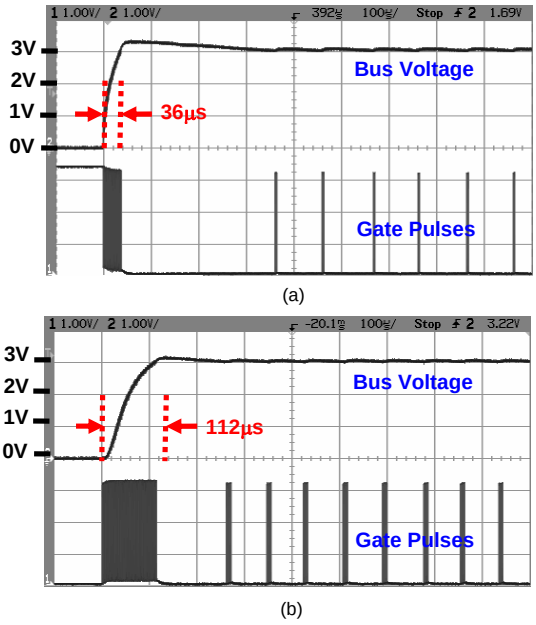

Figure 4. Start-up response of the SC DC-DC converter: (a) when input voltage = 3.3V, (b) input voltage = 2.6V

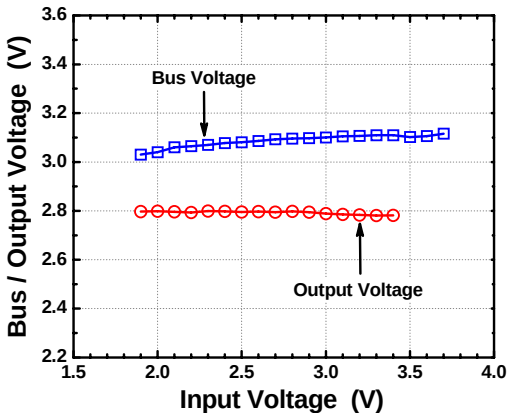

Figure 5. Variation of output voltage with input voltage (f_s = 5MHz)

The output voltage is monitored with the converter system subjected to varying load. Fig. 7 shows the response of the system when the load varies. It is observed that the output is stable up to 27mA of load current, after which the output starts to droop. The converter system is also tested with load transients. The load transients are generated by switching the load resistances. Fig. 8

shows the response of the system when subjected to a load transient from 2mA to 20mA and vice-versa. Due to large equivalent series resistance (ESR) present in our circuit, relatively large overshoots are observed. Nonetheless, the output voltage recovers in less than 500ns.

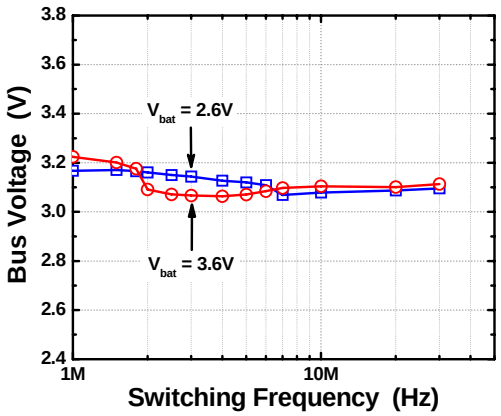

Figure 6. Effect of switching frequency on the bus voltage for buck (V_{bat}=3.5V) and boost (V_{bat}=2.6V) mode of operation

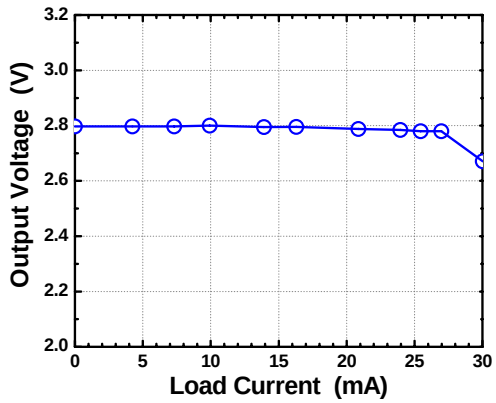

Figure 7. Output voltage with varying load

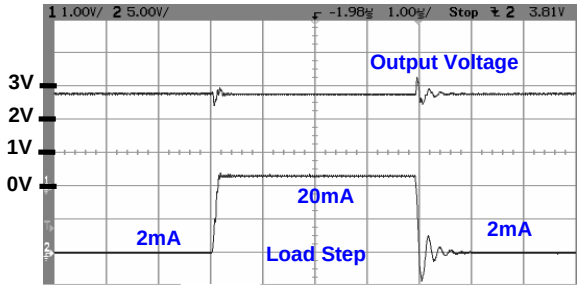

Figure 8. Experimental results showing the response to load transients

The fabricated chip was tested over a range of supply voltages and load currents. The summary of the measurement results is shown in Table I together with the results from other works. The presented buck-boost hybrid DC-DC converter is favorably compared with others. For low load currents, the proposed architecture provides a good alternative to the conventional buck-boost DC-DC converter without requiring any inductive element or a complicated reconfigurable network of switches and capacitors.

TABLE I. SUMMARY OF PERFORMANCE COMPARISON

Parameter	[7]	[3]	[2]	This work
Technology	0.6µm	0.13µm	0.35µm	0.18µm
Chip Area (mm^2)	3.92	4.00	0.65	2.49
Input Voltage	1.5V to 2.5V	1.2V	2.0V to 4.0V	2.4V to 3.6V
Output Voltage	3.0V to 5.0V	0.7V and 2.1V	16V	3V
Conversion Ratio	2	2, 0.66	8–4	0.8–1.2
Switching Freq.	500kHz	23MHz	50kHz	30MHz
Flying Capacitor	1µF	1.2nF	0.47µF	1µF
Output Capacitor	2.2µF	N.A.	0.47µF	1µF
Maximum Current	<50mA	~2.3mA	11.2mA	27mA
Quiescent Current (@2.5V)	1.63mA	N.A.	0.49mA	0.212mA
Maximum Efficiency	>90%	66% @1.4mW	N.A.	58.5% @6mW

IV. CONCLUSION

A hybrid buck-boost DC-DC converter was designed and fabricated. A simple hysteretic voltage control was used to regulate the bus voltage, which is down-converted to the required output voltage by the linear regulator. The proposed converter topology does not require any bulky magnetic elements and does not rely on changing the voltage gain of the SC DC-DC converter. The measured results show that the proposed scheme can be used for low-power battery-operated applications which require the regulated supply voltage with low ripple.

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