A Digital Programmable Sensor Interface Circuit for Wide Range Silicon Nanowire Pressure Sensor

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***Abstract* — This paper presents a sensor interface circuit for silicon-nanowire (SiNW) pressure sensors. The sensor interface circuit can be used for a sensorized guidewire in minimally invasive vascular surgery and blood flow sensor in prosthetic vascular graft. The sensor interface circuit converts resistance of the SiNW sensors to a fully differential analog voltage. It consists of a multiplexed switched current integrator followed by a programmable gain stage. There are two major challenges: limited power from wireless link and huge resistance variation of the SiNW sensor. These challenges are addressed through a multiplexed switched current integrator with programmable integration time and switched capacitor gain stage. The chip has been fabricated in 0.18μm CMOS technology, occupies an area of 470μm × 310μm, and consumes 180 µW at 1V supply.**

***Index Terms* — Sensor interface circuit, Switched current integrator, Switched capacitor gain stage, Resistance to voltage conversion.**

I. INTRODUCTION

In many bio-implanted devices and sensor nodes, sensor interface circuit is required to translate the change in sensor property to a signal that can be processed by the next stage of sensor system. One type of sensors that can be used for such devices and systems is piezoresistive sensors. In [1], we implemented SiNW piezoresistive transduction method for force sensing for sensorized guidewire and blood flow sensor.

In the guidewire application, insertion of catheter into a blood vessel is required in endovascular catheterization procedure as a minimally invasive surgical operation. By threading the catheter into the circulatory system, the location and amount of blockage present in major vessel can be determined. The affected area can also be accessed for treatment by the specialist. However, for successful passage of the guidewire through the narrowing vascular vessel, skill and precision of the surgeons are required [2]. Therefore, sensorized guidewire to help the surgeons understand the passage to navigate through the vessel during the procedure is needed.

Figure 1 shows the application of the sensorized guidewire during endovascular catheterization procedure. A miniaturized microelectromechanical system (MEMS) force sensor is mounted at the tip of the guide wire. The force sensor is sensitive to detect force within the safe margin to avoid blood vessel damage. With the SiNW used as the MEMS sensor, high sensitivity sensor is possible to achieve. This miniaturized device requires ASIC (Application Specific Integrated Circuit) that is small in size.

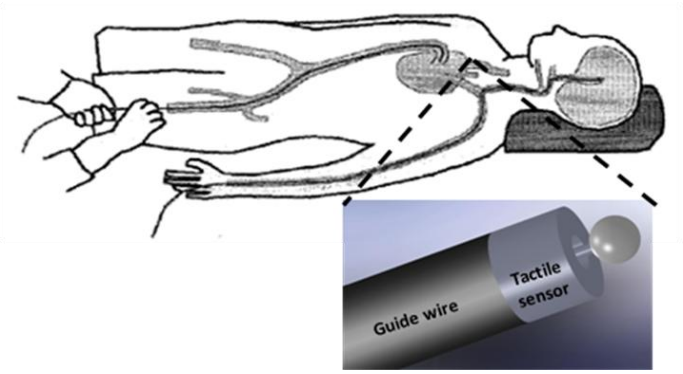

Figure 1. The application of sensorized guidewire in endovascular catheterization procedure [1]

Blood flow sensor in a prosthetic graft is another application of pressure sensor. Prosthetic grafts are frequently used in vascular surgery in the context of bypass surgery for lower limb ischemia or as a conduit for haemodialysis in renal failure. In these settings, graft failure can result in deleterious outcomes for the patients i.e. worsening ischemia, inability to undergo haemodialysis. Insufficient blood flow rates in these grafts are predictive of subsequent graft thrombosis and failure. Underlying this is the presence of stenoses in the graft or downstream from the graft. Variations in flow rates can localize the position of significant stenoses that may result in graft thrombosis. Flow rate monitoring provides an indication for early intervention to prevent graft failure.

In Figure 2, an implantable blood flow sensor device consisting MEMS based sensor, ASIC, and wireless power link is shown. Blood flow velocity in the prosthetic graft can be measured by the sensor, processed by ASIC and read with wireless link. Continuous monitoring of the blood flow over long period requires that the device have enough power source. In this work, we use wireless, inductive coupling as the power source. However, the power available from wireless link is very limited. Therefore, a low power front end interface circuit is needed.

In this work, we present a sensor interface circuit to translate the change in sensor's resistance to a fully differential analog voltage. SiNW piezoresistive sensors with nominal resistance from 20kΩ to 800kΩ are used in this work to sense

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the blood flow and guide-wire pressure. In flow sensor, the output resistance changes according to the blood flow velocity, while in tactile sensor, the output resistance changes according to the pressure asserted at the tip of the sensor.

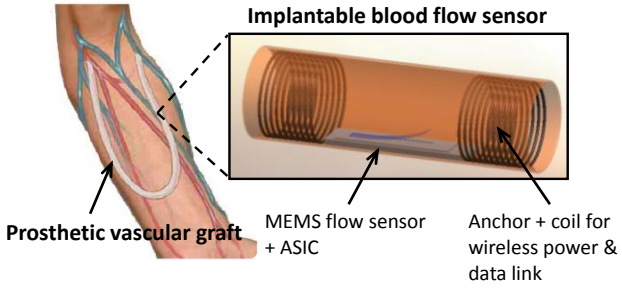

Figure 2. The prosthetic graft with the sensor, IC, and coil

II. DESIGN METHODOLOGY

A multiplexed switched current integrator approach for the resistance to voltage conversion is presented in this paper. Figure 3 shows the system architecture of the sensor interface circuit. The sensor interface circuit consists of four channel sensors, channel selection/timing generation/gain selection block, multiplexed switched current integrator and single ended to fully differential programmable gain stage. The basic idea of the proposed sensor interface circuit architecture is to convert the resistance of the sensor to a fully differential analog voltage. The multiplexed switched current integrator converts the sensor's resistance to current, and integrates it to a final voltage. The single ended output voltage is amplified and converted to a fully differential analog voltage.

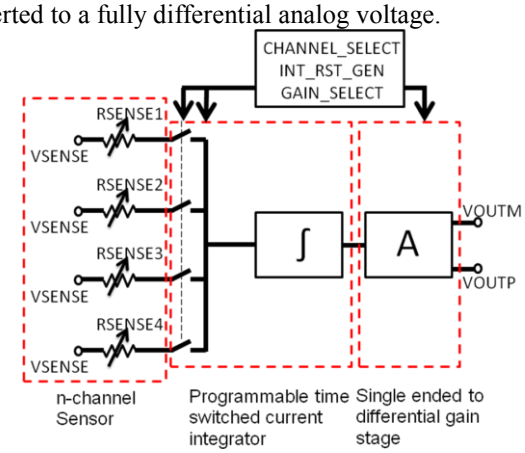

Figure 3. The architecture for the sensor interface circuit.

This architecture is attractive because a wide range of resistance can be covered by changing the integration time as shown in Figure 4. Multiple sensor channels can also be time-multiplexed easily. In [3], a current Digital to Analog Converter (DAC) was deployed to cover the wide range of resistance. However, the largest resistance that can be covered is limited by the Least Significant Bit (LSB) current. Our approach is limited by the maximum integration time. Large resistance is covered by longer integration time at the expense of lower conversion rate.

In our approach, a fixed voltage is applied across the sensor to limit the maximum current consumption of the sensor. The sensor's resistance is then converted to a constant current, which is integrated according to the preset integration time. The integrator output voltage is given by the equation

$$V_{OUT} = V_{CM,INT} + \frac{V_{CM,INT} - V_{SENSE}}{R_{SENSE} C_{INT}} \times T_{INT} \quad (1)$$

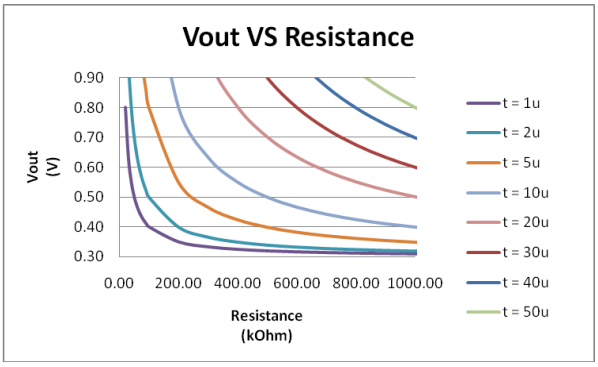

Figure 4. Integrator final voltage versus the resistance of the sensor.

where V_{OUT}, $V_{CM,INT}$, V_{SENSE}, R_{SENSE}, C_{INT}, and T_{INT} is the integrator output voltage, common mode voltage, sensor's voltage, sensor's resistance, integrating capacitor, and integrating period respectively. The integrator parameters such as V_{OUT}, $V_{CM,INT}$, V_{SENSE}, C_{INT} and T_{INT} has to be selected carefully in order to achieve the desired resistance range and error. A 100mV is applied across the sensor to minimize the integrator capacitance for reducing the chip area. V_{OUT} is targeted to be in the range of 700mV ± 50mV to keep the integrator's operational amplifier in saturation. Based on these parameters, the integration time versus resistance is plotted in Figure 5. From this plot, C_{INT} of 10pF is required to cover the range of the resistance (from 20kΩ to 800kΩ). Furthermore, T_{INT} can be programmable from 0.5μs to 64μs by a 7-bit digital control to accommodate this harsh sensing resistance requirement.

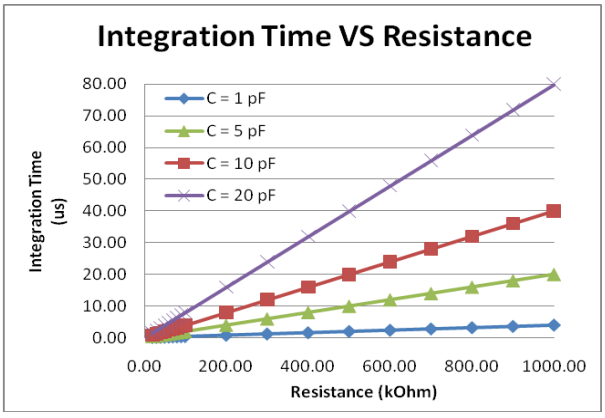

Figure 5. Integration time versus the resistance of the sensor for different integrating capacitor size.

At the end of integration, the final output voltage is held for the conversion to digital by an Analog to Digital Converter (ADC). However, since the dynamic range of the integrator is designed to be 100mV (from 700mV ± 50mV), this voltage is required to be amplified and converted to a fully differential voltage by a programmable gain stage to optimize the Signal to Noise Dynamic Range (SNDR) of the ADC. Switched capacitor gain stage architecture is applied in this chip to reduce the overall power consumption.

III. CIRCUIT BLOCKS

1. Multiplexed Switched Current Integrator

Figure 6 shows the one channel switched current integrator with offset cancellation circuit. Multiple channels can be time-multiplexed by connecting the sensors with individual switch SW_3 that controls the integration time and sensor channel selection.

The operation of the integrator can be explained as follows: During reset period (RST), switch SW_1 and SW_2 are closed while switch SW_3 is opened, making the operational amplifer (op-amp) in the unity gain configuration. The offset of the op-amp is stored in the capacitor C_{OFF} during this period. There is no current flowing through SW_1 since SW_3 is opened. Non-overlapping time between the reset and the integration period (pre-integration hold) ensures that SW_2 and SW_1 are fully opened before SW_3 is closed so that no input current is lost. Integration period (INT) begins when SW_3 is closed with SW_1 and SW_2 are open. The offset voltage that is stored in the capacitor C_{OFF} is now cancelled. Sensor's current flows and is integrated through the capacitor C_{INT} producing a linear positive ramp. The slope of the ramp depends on the sensor's resistance. At the end of the integration period, all switches are opened. During this period, the final output voltage is held by the integrating capacitor C_{INT}. The output voltage at the end of integration is proportional to the average input current throughout the integration period.

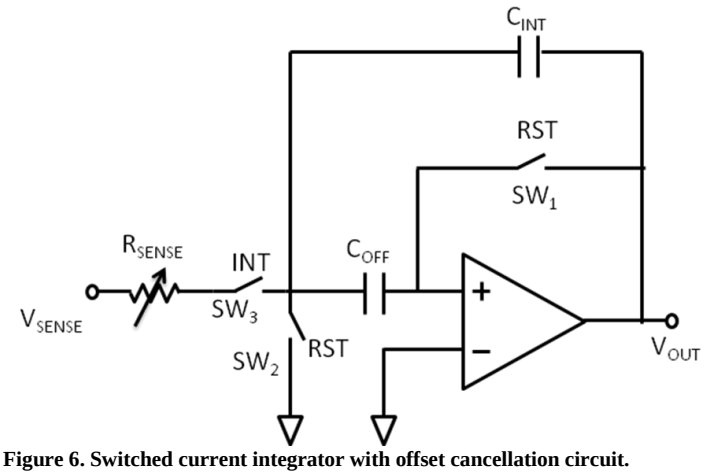

Figure 6. Switched current integrator with offset cancellation circuit.

During hold period, the droop rate of the 10pF integrating capacitor C_{INT} is slow enough that it does not contribute significant error during the gain stage sampling. The timing diagram and output voltage waveform is shown in Figure 7.

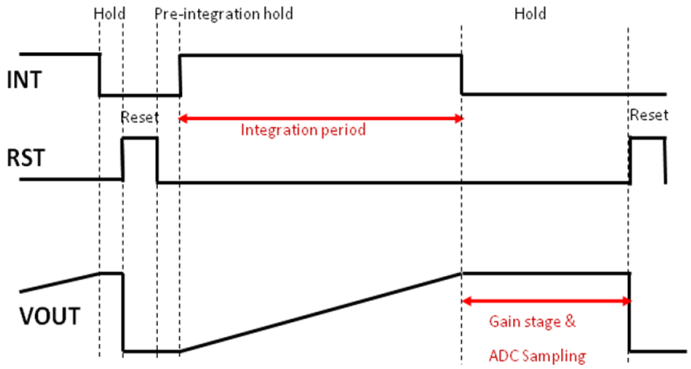

Figure 7. Timing diagram for the switched current integrator operation.

2. Gain Stage

The single ended output voltage from the integrator is required to be amplified and converted into a differential signal before it is digitized. This process can be achieved by applying a fully differential switched capacitor programmable amplifier, which is shown in Figure 8. The gain stage consists of a fully differential folded cascode opamp with an internal switched capacitor common mode feedback (SC-CMFB), a programmable switched capacitor (SC) feedback, and a non-overlapping clock generator. The gain of this stage is controlled by the programmable capacitor banks C_1. The operation of the gain stage is given as follows: During S_1, the input voltage is stored in term of charge in the capacitor C_1, the op-amp will hold the previous value while the charge at C_2 is reset. During S_2, the charge in C_1 is transferred to C_2. Then the cycle repeats again. Capacitor C_3 keeps the op-amp in closed loop and holds the previous voltage. However, it does not contribute the gain of this stage which is given by C_1/C_2.

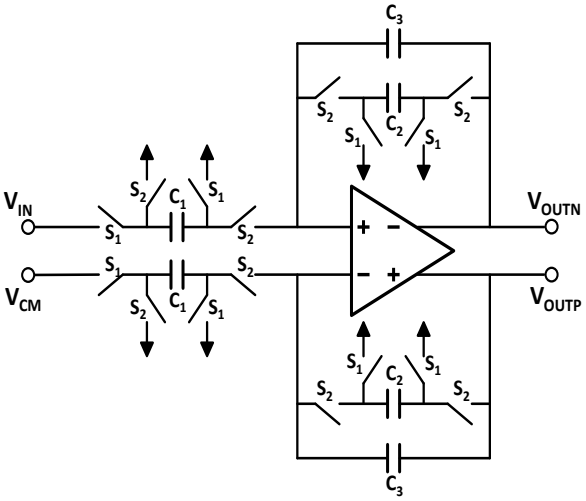

Figure 8. Switched Capacitor Programmable Gain Amplifier.

IV. MEASUREMENT RESULTS

The sensor interface circuit was fabricated using 0.18μm CMOS technology and occupies an area of 470μm × 310μm. It consumes 180μW from a 1V power supply. Based on simulations, the sensor interface circuit consumes only 22% of the total power. Four channel sensors are multiplexed in the fabricated chip to test the time-multiplexing scheme. The timing control of the sensor interface circuit was implemented by a Field Programmable Gate Array (FPGA) board. Figure 9 shows the output waveform of the integrator.

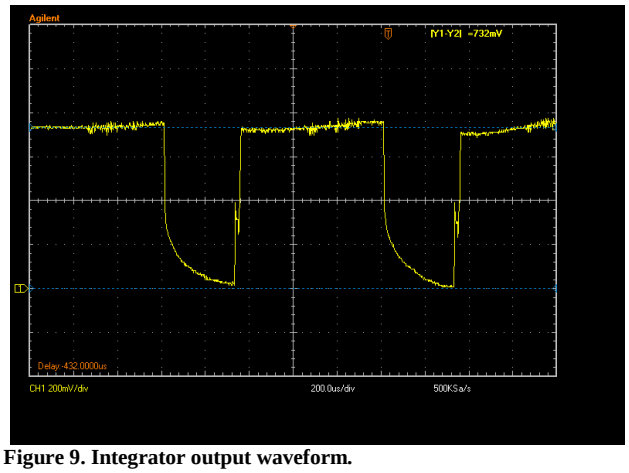

Figure 9. Integrator output waveform.

Figure 10 shows the integrator output voltage versus the inverse of sensor's resistance for different resistance range and integration time. The measurement was carried out by adjusting the ratio of R_{SENSE}/T_{INT} such that the integrator's output voltage is within the specification, which is 700mV ± 50mV.

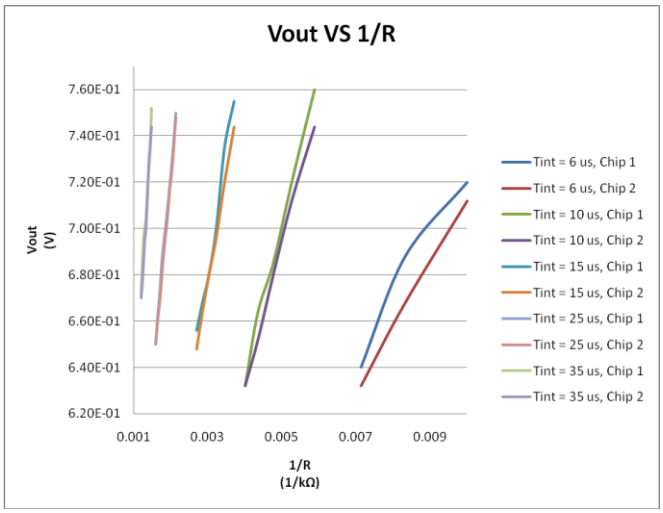

Figure 10. Integrator output voltage versus inverse of sensor's resistance.

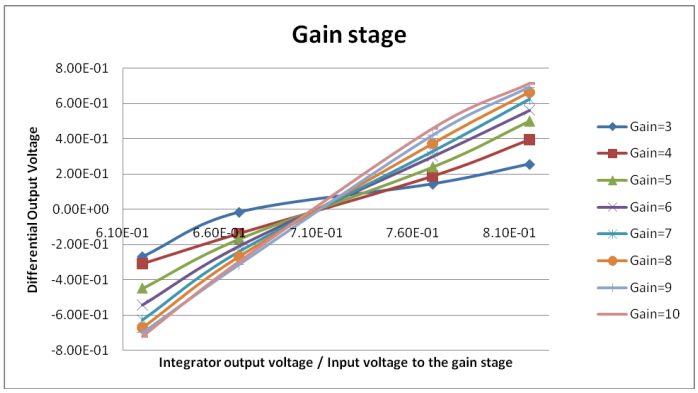

Figure 11. Gain stage characteristic.

Figure 11 shows the gain stage characteristic. The PGA can be programmed through the 3-bit capacitor bank to give the gain of 3 to 10. At lower gain settings, there is gain error caused by the small size of the capacitor C_1 and C_2. However, since the gain stage is used to maximize the input voltage to ADC, this nonlinearity can be easily compensated through digital calibration.

V. CONCLUSIONS

A sensor interface circuit for SiNW pressure sensor and flow sensor is presented. Multiplexed switched current integrator architecture is selected to convert input sensor's resistance to an analog voltage. Wide range resistance is covered by the 7-bit programmable integration time. The sensor interface circuit consumes 180μW from the 1V supply.

ACKNOWLEDGMENT

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