A process tolerant analog ASK baseband for UHF RFID reader and implantable applications

M.Kumarasamy Raja and Xuesong Chen
Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 11 Science Park Road, Singapore Science Park II, Singapore 117685

***Abstract*— An envelope generation circuit which generates the top and bottom envelope for PR-ASK, SSB-ASK and DSB-ASK with modulation depths (*m*) from 10% to 100% with steps of 10% for use in EPC and ISO compliant RFID reader is described. It employs a V_{TH} independent level shifter biased with a V_{TH} tracking circuit so that the change in V_{TH} due to process variation does not distort *m*. The highest level shifter error is 7% under extreme PVT when the V_{TH} varies by 63%. Measured results include a modulation depth accuracy of 2%, modulation steps of 10% under supply and temperature extremes.**

I. INTRODUCTION

Amplitude Shift Keying (ASK) is the preferred modulation scheme for UHF RFID readers and inductive links to implants as it can provide the dc power required for the tags and implants in addition to easier envelope detector based demodulation. DSB-ASK with modulation depths (*m*) varying from 18% to 100%, PR-ASK (suppressed carrier) and SSB-ASK are recommended for RFID reader to tag link. EPC Global recommends DSB-ASK with *m* from 20% to 100% for class-0 (passive) tags [1] whereas ISO needs 27% to 100% for type A and 18% to 100% for type B tags [2]. Lower *m* provides more average power with lowest ripple and is useful for battery less tags and implants. Lower ripple also helps to avoid (or reduce the size) the bulkier RC filter in the implants and tags. On the other hand *m*=100% gives maximum SNR and is useful at short range [2]. PR-ASK (suppressed carrier) and SSB-ASK are recommended for class-1 tags in single channel and multi channel environment [1].

All the three modulation formats, are conventionally realized by performing the digital operations (details in sec. IIA) and then applying to a double balanced Gilbert cell mixer (DBM) through a Digital to Analog Converter (DAC) [3]. In order to meet the strict transmission mask in dense reader environment DAC output is to be filtered well needing a pulse shaping filter (PSF) after the DAC as shown by the dashed portion of Fig. 1. The digital baseband processing is either carried out through a microcontroller off chip [3] or is carried out on chip with memory option [4]. To reduce cost of the reader module, this paper demonstrates an analog method of generating the envelope which has been integrated as an additional parallel option to the conventional scheme in [3]. Proposed circuit also obviates the need for the DAC and PSF as the analog signal does not contain spikes, reducing the power consumption, chip area and the cost further.

Reported analog ASK modulators cater only for single value of *m* [5]. This paper describes an ASK envelope generator which when used with a double balanced mixer (DBM) shown in Fig. 1 generates all the forms of modulated output required for UHF RFID reader, viz, DSB-ASK with *m* varying from 10% to 100% with a step of 10%, PR-ASK and SSB-ASK.

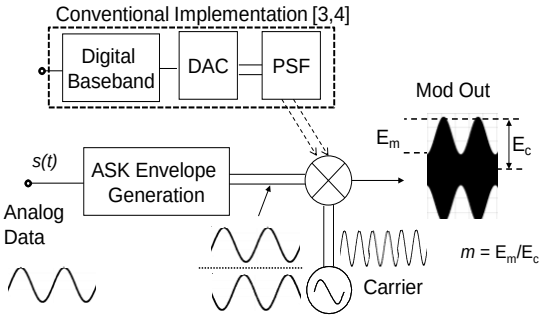

Fig. 1 ASK generation using a doubly balanced Gilbert cell and the proposed ASK envelope generation circuitry

II. ASK BASE BAND

A. ASK Envelope Analysis

Modulated signal at the transmitter is given by

$$y(t) = x(t)\cos\omega_0 t \quad (1)$$

x(t) is the envelope and takes different forms based on the selected modulation. For PR-ASK x(t) is equivalent to the incoming bipolar signal as below.

$$x_{PRASK}(t) = s(t) \quad (2)$$

s(t) takes on values -1 or +1 depending on the incoming data with a mean value of zero. Phase of the modulated carrier is reversed for every bit change resulting in zero carrier energy and maximal modulating signal and hence maximum SNR.

In case of DSB-ASK, the envelope allows certain amount of carrier to be transmitted depending on the value of *m* such that

$$x_{DSB\text{ - }ASK}(t) = [(1-m) + m \times s(t)] \quad (3)$$

Thus, the higher the *m*, the higher the signal to carrier power. In (3) *s(t)* takes on values 0 to 1 depending on the incoming data(unipolar). Although the SNR for the given transmitter power is low for lower *m* it permits rectification without the use of RC filters reducing the size of implants and tags.

SSB-ASK is the most bandwidth efficient option and is used in the dense reader circumstances. The envelope of the SSB-ASK signal is complex consisting of both I and Q terms as below.

$$x_{SSB\text{ - }ASK}(t) = [s(t) + j\,\hat{s}(t)] \quad (4)$$

Proceedings of the Second APSIPA Annual Summit and Conference, pages 733–736,
Biopolis, Singapore, 14-17 December 2010.

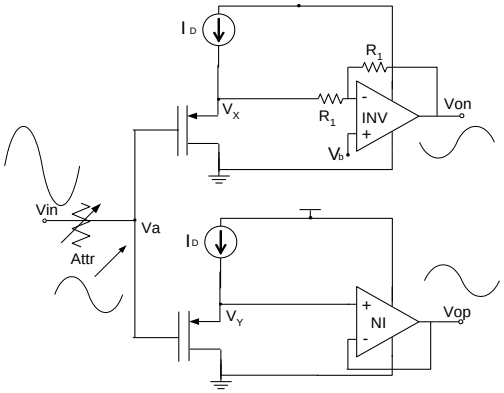

Fig. 2. Circuit Diagram of the ASK envelope Generator

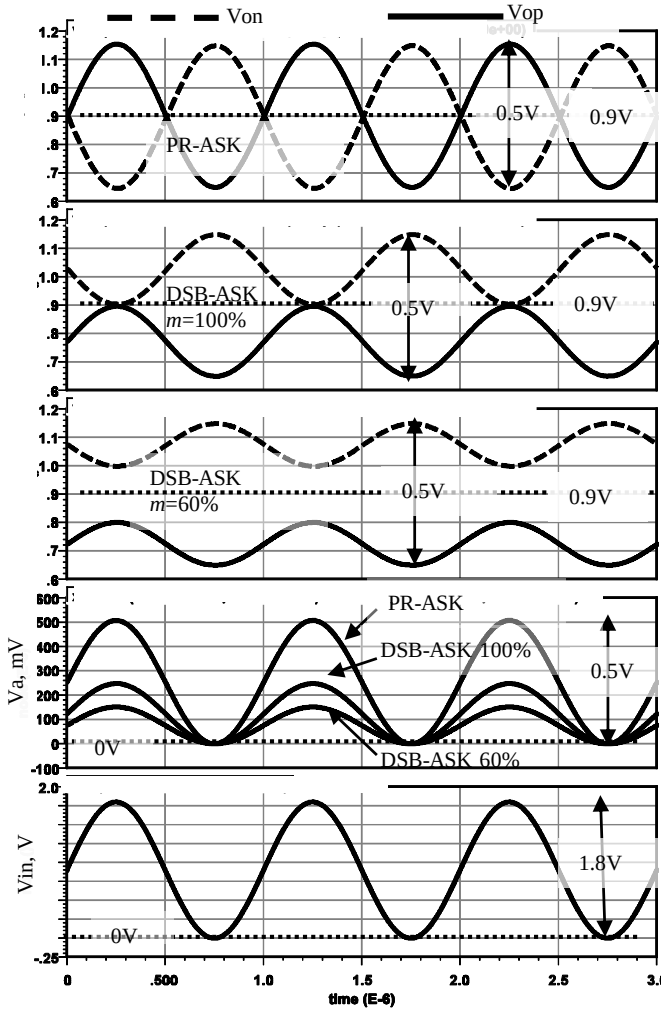

Fig. 3 Waveforms at different nodes. Top 3 curves are the outputs or envelopes for PR-ASK, DSB-ASK with *m*=100 % and *m* = 60 % respectively.

Hence, two chains (I and Q) are employed for SSB-ASK. $\hat{s}(t)$ is the Hilbert transform of the input signal *s(t).* Often this Hilbert transform is not performed on the base band. Rather the LO signal which forms the second input is applied as a complex signal. The LO in the reader anyway provides I and Q outputs for the receiver chain be it low IF or zero IF [3]. Hence, a real signal *s(t)* is multiplied with complex LO to obtain the modulated signal [3,4]. ASK baseband generates the envelope signal *x(t)* as described in equations (2) to (4).

B. ASK Envelope generation Circuity

Fig. 2 shows the circuit schematics of the proposed ASK envelope generator. Corresponding waveforms are shown in Fig. 3. Top 3 waveforms are the envelopes *x(t).* Analog base band is first passed through a programmable attenuator, the settings of which determine the type of modulation and the modulation depth (*m*). The input signal which varies from 0 to VDD (1.8 V), is attenuated to 500 mVpp (Attenuation factor α = 0.5/1.8) for PR-ASK, then level shifted to 0.9 V by the PMOSFETs and then amplified by the op-amp based inverting and non-inverting amplifiers with a gain of unity to get the two envelopes. Common mode voltage is maintained at VDD/2 by the op-amps so that the outputs are balanced as shown by the top waveform in Fig. 3. For DSB-ASK with a modulation depth of 100%, input signal is attenuated to 250 mVpp (α = 0.25/1.8) and the waveform is shown by the second from top. For *m* < 100%, the attenuator is programmed to give *m**250 mVpp (α = *m**0.25/1.8), so that the amplitude is *m* times the carrier amplitude. Waveform for *m* of 60% is shown for illustration. In case of SSB-ASK the operation is similar to PR-ASK but two arms (I & Q) are used as discussed in section IIA. The op-amps consume a current of 90µA each. The driving capabilities were over budgeted so that the gilbert cell remains linear as all the modulations schemes are non-constant envelope type.

C. Modulation Distortion Issue due to Vth variation

The outputs Vop and Von are equal in amplitude, opposite in phase but not purely differential in the sense that the dc level of V_{op} and V_{on} vary based on *m*. Hence, level shifting from Va to V_X and V_Y with a dc voltage of VDD/2 needs to be accurate otherwise modulation distortion will result. Fig. 4 (a) and (c) illustrate the modulation distortion for in fast-fast (FF) and slow-slow (SS) process corners respectively. The curve in the middle, Fig 4(b), shows the ideal envelope for DSB-ASK with *m*=100% which is met in the typical condition. Any deviation from the ideal envelope causes distortion and can be expressed in %. In case of FF corner, lower V_{th} (and hence V_{GS}), reduces the dc levels of V_X and $V_{Y.}$ The two output waveforms move away from each other causing carrier leakage in the modulated signal. In the SS corner higher V_{th} (and hence V_{GS}), increases the dc levels of V_X and $V_{Y,}$ which causes the two output waveforms to overlap. Modulation distortion is about 40%, much more than the 10% step desired. V_{GS} variation is due to the change in V_{th} of the PMOSFETs related to the constant current I_D as below.

$$I_D = \frac{\mu_p C_{OX}}{2}\frac{W}{L}(|V_{GS}| - V_{th})^2 = \frac{\beta_p}{2}(|V_{GS}| - V_{th})^2 \qquad (5)$$

V_{th} in a typical 0.18-µm CMOS process varies by about 250 mV under process and temperature extremes. DC levels of V_X and V_Y are shifted by the varying V_{th} levels. This is high compared with the magnitude of every step (10%) for the

DSB-ASK which is 25 mV and limits the minimum *m* achievable. To solve this issue either a calibration scheme for I_D or a circuitry which keeps the V_{GS} constant irrespective of variation in V_{th} is desired. We have used a biasing circuitry which keeps the V_{GS} constant as will be seen in next section.

D. Proposed constant level shifter

Fig. 5 shows the proposed biasing details for the PMOS level shifter. The drain current I_D is derived from the MOSFET potential divider consisting of M_1, M_2 and M_3 and tracks the V_{th} variations. Since the drain current through M_1, M_2 and M_3 are same:

$$\frac{\beta_1}{2}(|V_1 - V_{DD} - V_{th1}|)^2 = \frac{\beta_2}{2}(|V_2 - V_1 - V_{th2}|)^2 = \frac{\beta_3}{2}(|V_2 - V_{th3}|)^2 \quad (6)$$

Eliminating V_2 in (6), noting that $\beta_2 = \beta_3$ and $V_{th2} = V_{th3}$ we get,

$$V_1 = \frac{\sqrt{\frac{\beta_1}{\beta_2}}(V_{DD} - V_{th1}) + V_{th2}}{0.5 + \sqrt{\frac{\beta_1}{\beta_2}}} \quad (7)$$

By making β_1 smaller than β_2, V_1 increases fractionally with *Vth*. Table 1 shows the simulated values of different node voltages at process temperature extremes. Variation in V1 is only 7% when compared with the variation of 63% in Vth. The level shifter is made PMOS only so that it is not affected in the complementary (slow-fast SF and fast-slow FS) corners.Table 1 shows the simulated values of different node voltages at process temperature extremes. Variation in V1 is only 7% when compared with the variation of 63% in Vth. The level shifter is made PMOS only so that it is not affected in the complementary (slow-fast SF and fast-slow FS) corners.

III. MEASUREMENT RESULTS

The proposed ASK envelope generator with a test buffer was fabricated in 0.18-µm 1P6M (single poly six metal) CMOS process and operated with a supply voltage of 1.8 V. The chip microphotograph is shown in Fig. 6. The ASK envelope generator occupies an area 160µm × 160µm and the test chip occupies an area of 1mm × 1 mm . It was bonded to a DIP 24 package and assembled on a FR4 PCB. Table II shows the summary of measured results. All settings of *m* from 0% to 100% were measured. Worst case distortion was observed at *m*=70% (Fig. 9). Figure 10 shows the spectrum of PR-ASK envelope which has the maximum signal swing of 1Vpp (differential) and the THD is better than 45 dB at 1 MHz.

TABLE I
LEVEL SHIFT FOR PROCESS AND TEMPERATURE VARIATION

Corner/ Temp	β_1	β_2	β_3	V_{th} (mV)	V_1 (V)	Vgs4 (mV)
SS /-40	2.78	7	7	535	1.17	620
TYP/25	2.21	5.6	5.6	387	1.13	650
FF/75	1.92	4.9	4.9	291	1.1	667

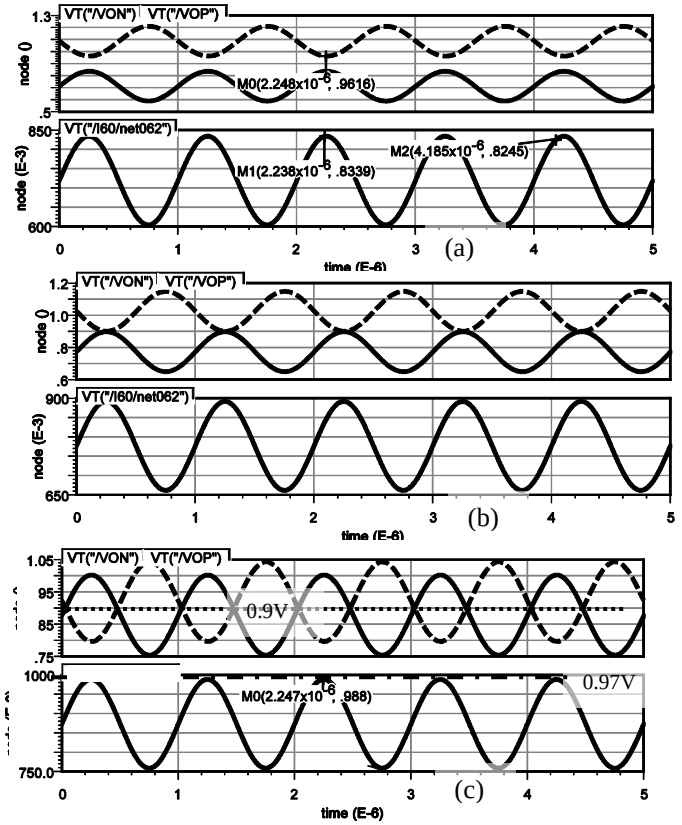

Fig. 4 Signal at the output of level shifter (Vx and Vy) and outputs of DSB-ASK with *m*=100 %. (a) fast-fast case DC level of Vx and Vy reduced resulting in carrier leakage (b) Typical case and (c) slow-slow case DC level of Vx and Vy increased resulting in modulation distortion

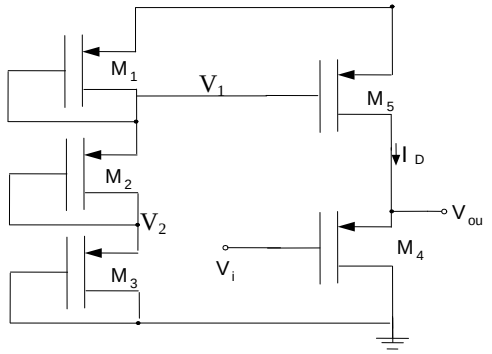

Fig. 5 PMOS level shifter with level shift independent of V_{TH}.

TABLE II
SUMMARY OF MEASURED RESULTS

Modultion schemes	PR-ASK (suppressed carrier), DSB-ASK(with carrier), SSB-ASK
Modulation depth	100% to 10% at 10+/-2% step
Input signal amplitude	0 to VDD single ended
Output voltage	0.5Vpp SE (1Vpp diff)
THD	Better than 45 dBC (under all options)
Data rate	40 kbps/80 kbps /160kbps
Technology	0.18-µm CMOS
Power consumption	1.8V × 280 µA

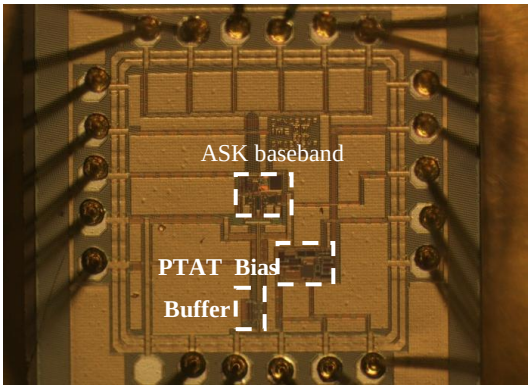

Fig. 6 Chip Micrograph of the test chip.

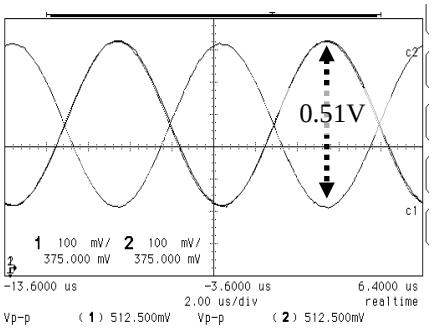

Fig. 7 Measured PR-ASK envelope for 1 MHz input.

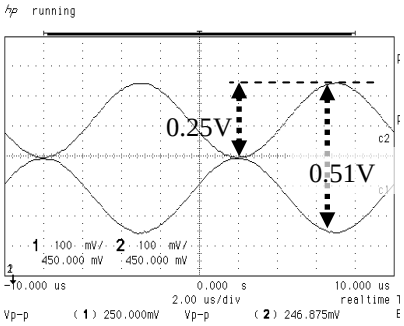

Fig. 8 Measured ASK with 100 % modulation depth for 1 MHz input.

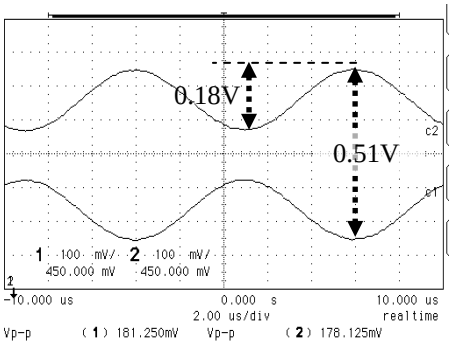

Fig. 9 Worst case modulation distortion measured at 70% modulation depth.

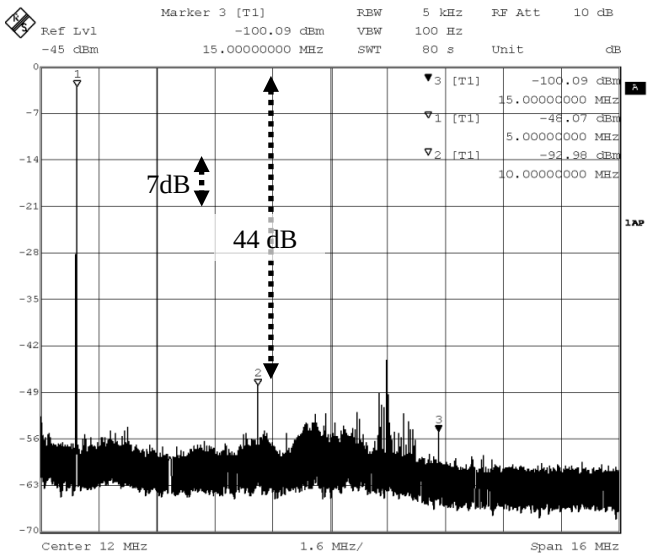

Fig. 10 THD in the PR-ASK waveform which has the maximum output swing of 1 Vpp (diff)

IV. Conclusions

A cost effective and power efficient analog solution for generating the envelope of PR-ASK, SSB-ASK and DSB-ASK modulation for modulation depths from 10% to 100% with steps of 10% was described. A V_{th} independent level shifter biased with a V_{th} tracking circuit ensures that the change in V_{th} due to process variation does not distort the modulation depth. The highest simulated level shifter error is 7% under extreme PVT when the V_{TH} varies by 63%. It demonstrates a modulation depth accuracy of 2% for modulation steps of 10 % under supply and temperature extremes. The reader chip which uses the proposed ASK baseband have been tested for mask (ETSI/FCC) and standard (ISO/EPC) compliance and has been commercialized.

References

[1] EPC Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz—960 MHz, Version 1.0.9, Jan. 2005.

[2] INTERNATIONAL STANDARD ISO/IEC 18000-6, First edition Aug 2004 Information technology Radio frequency identification for item management Part 6:

[3] Khannur, P.B *et. al.*, "A Universal UHF RFID Reader IC in 0.18-µm CMOS Technology, " *IEEE J. Solid-State Circuits*, vol. 43, Issue 5, May 2008 pp. 1146 - 1155

[4] I. Kwon, H. Bang, K. Choi, S. Jeon, S. Jung, D. Lee, Y. Eo, H. Lee, and B. Chung, "A single-chip CMOS transceiver for UHF mobile RFID reader," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 729–737, Mar. 2008.

[5] Y-D Lee *et. al.*, " ASK modulator for RFID system using a novel variable DGS resonator, " *Proc. Of the 4th European radar conference* Oct 2007, pp.381-384.