A Low-Voltage Low-Power Sigma-Delta Modulator for Biomedical Application

V.Navaneethan and Yuanjin Zheng
Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore.

***Abstract*—A low-voltage low-power discrete time sigma delta modulator for biomedical signal acquisition designed and implemented in 0.18-µm CMOS process is presented in this paper. This sigma delta modulator is designed using cascaded 3rd-order feedback form of integrator with the over sampling ratio (OSR) of 32. The experimental prototype chip achieves 55dB and 60dB dynamic range for 200Hz and 500Hz signals respectively. It consumes 20µW power from a 1Volt power supply**.

I. INTRODUCTION

Sigma-delta analog-to-digital converters (ADCs), initially used for audio-band and high resolution applications, are now widely used in systems requiring video-band and medium-resolution. This technique benefits from both noise-shaping and over sampling to give an optimum trade-off between speed and resolution.

The modualator was used in ECG signal acquisition platform followed by a post decimation filter. The purpose of the system is to provide analog-to-digital conversion. Sigma-delta type ADC is selected due its potential usage of digital processing techniques, scalability and adaptability for different Bio-signal such as ECG and EEG [1]. Sigma-delta ADCs employing noise shaping techniques have been widely used because they provide an effective means to achieve a high resolution without the need for high-precision analog circuits. In particular, single-loop 1-bit sigma-delta ADCs has been popular for their simplicity and insensitivity to imperfections of analog circuits [2], [3]. However, single-loop structures are not attractive for high-order [2] modulation because of stability concern. Although a single-loop higher-order modulator can be stabilized using various techniques, they results in loss of performance, in general. A popular way to realize a stable high-order modulator is to use a multistage or cascaded structure [4]. Cascaded structures, however, are prone to noise leakage due to mismatch among modulators and the noise-cancellation filter, which calls for digital correction [4]. An alternative approach for a stable modulator is to employ a multibit quantizer. The multibit quantizer not only reduces the quantization noise power, but it also it improves stability of the modulator. The main drawback of using a multibit quantizer is stringent linearity requirements placed on the feedback digital-to-analog converter (DAC). The accuracy of the DAC needs to be as good as the overall modulator, necessitating digital correction or dynamic element matching [4]. The modulator requirements and specifications for individual sub blocks are derived from system level simulation in Matlab and architecture used in this work given below in Fig.1.

II. SYSTEM LEVEL SIMULATION IN MATLAB

Fig.1 shows the MATLAB system level model of cascaded integrator feedback type sigma delta modulator. Fig.2 shows the equivalent switched capacitor realization of Fig.1. Modeling and simulation are primary steps in the design cycle of mixed signal systems. In the design of sigma-delta modulator these steps become critical importance. Therefore, in this paper we performed exhaustive behavioral simulations taking into account most of the non-idealities, such as kT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate and saturation voltages).The most important noise sources affecting the operation of a sigma-delta modulator are the thermal noise of the sampling switches and the intrinsic noise of the operational amplifier. The total noise power of the circuit is the sum of the quantization noise power, the switch noise power and the op-amp noise power. Because of the large low-frequency gain of the first integrator, the noise performance of a sigma-delta modulator determined mainly by the switch and op-amp noise of the input stage [4]. These effects are simulated with MATLAB SIMULINK. This modulator was designed to achieve 50-60 dB SNR and SFDR of 50 dB over a bandwidth of 500Hz. The switching clock is derived from an on chip clock generator which gives choice on OSR of 32. Based on the Matlab simulation, 3rd-order single bit sigma-delta modulator was chosen as candidate architecture.

III. CIRCUIT DESIGN

A. *Current Mirror Operational Transconductance Amplifier (OTA)*

One of the most important building blocks in analog circuits is the amplifier. In modern sub-nanometer CMOS technology, the power supply voltage drops to one volt, but the threshold voltage is not scaled same proportion.Therfore, for low voltage application, it is desired to use less number of transistors in single stack. The current mirror OTA is used as shown in Fig.3, which uses less number of transistors in single stack and no need to drive compensatation capacitor, thus gives more power efficiency as compared to two stage counterpart. This fully differential OTA can achieve 50dB gain which is sufficient for system requirements.

Proceedings of the Second APSIPA Annual Summit and Conference, pages 749–752,
Biopolis, Singapore, 14-17 December 2010.

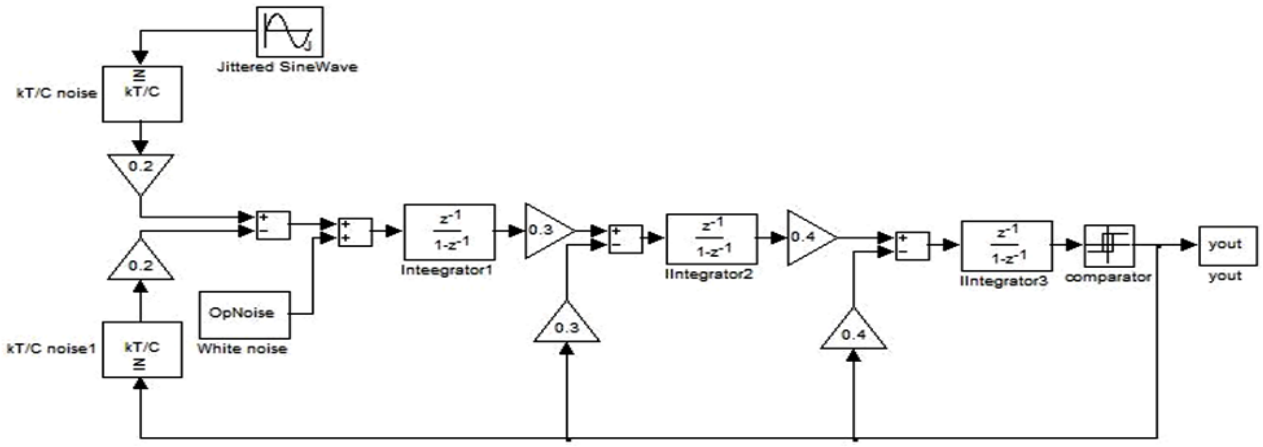

Fig.1. System architecture

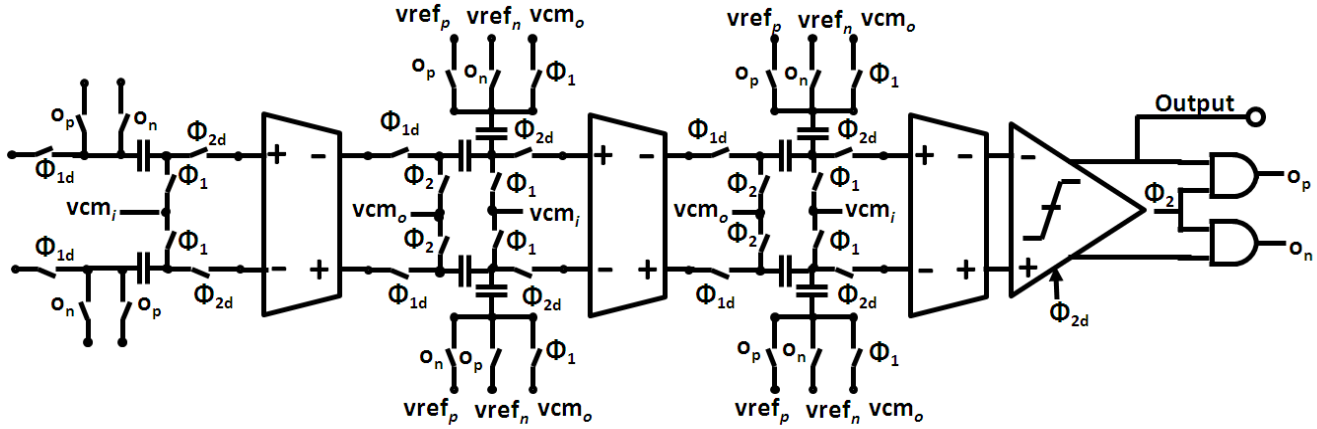

Fig.2. Switched Capacitor realization of Modulator

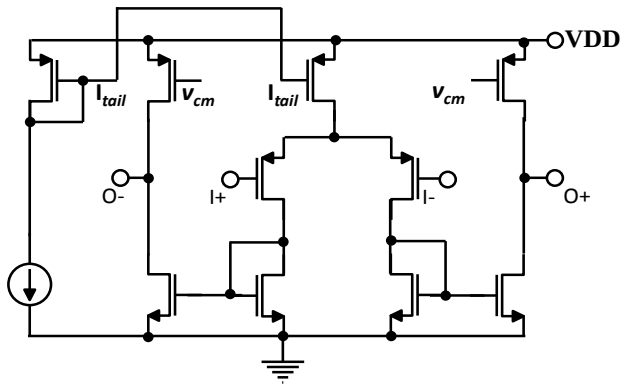

Fig. 3. Fully Differential Current Mirror OTA

B. *Switched capacitor common mode feedback (CMFB)*

Common-mode feedback (CMFB) is necessary in fully differential OTA and operational amplifiers to stabilize the common mode level at high impedance node. In current mirror OTA, there is one high impedance node at the output. Therefore, only one CMFB circuitry is enough to stabilize the output DC. The common-mode feedback circuit is implemented using switched-capacitor circuits. The transmission gates cannot be directly used as switch for switched-capacitor circuit, if supply voltage below the sum of the threshold voltage of NMOS and PMOS. Therefore, an alternate approach is required. In this work, we adopted bootstrapped switch reported in [5] shown in Fig.4. This switch was designed to operate at low-voltage with device reliability considerations. MOS transistors M1, M2 together with C1 and C2 form a clock multiplier. This will generate an over drive of 2*Vdd to gate of M3, therefore C3 can be charged up to Vdd. The accumulated charge in C3 will act as a floating battery to provide constant Vgs to switch transistor (M11) through M7 and M10. This switch is also used in CMFB circuitry and switched capacitor integrators.

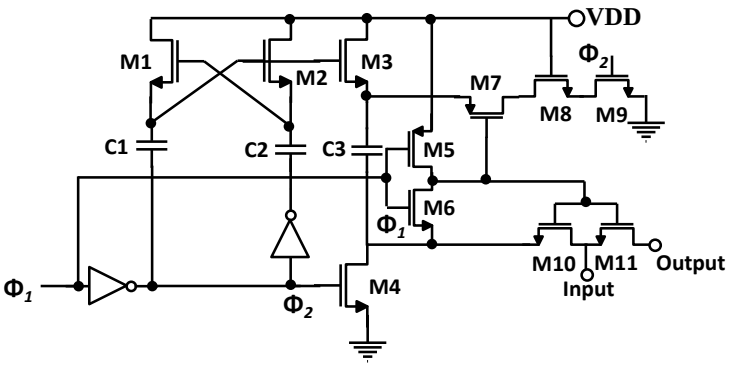

Fig. 4. Bootstrapped Switch used in CMFB and switched capacitor integrator

C. *Track and Latch comparator*

The offset voltage is one of the major non-idealities in comparators. Multi-bit quantizer requires very low offset preamplifiers to amplify the signal for accurate comparison. This will increase power consumption. Therefore, the single-bit quantizer is realized with a dynamic comparator followed by a SR latch as shown in Fig.5 is used. The comparator is a purely dynamic circuit, which consumes low power [6]. For a single-bit modulator, the requirement for the quantizer is quite relaxed as it is inherently linear and any non-idealities in this stage will be suppressed. Dynamic comparator's offset voltage can be reduced by matching of the input transistors.

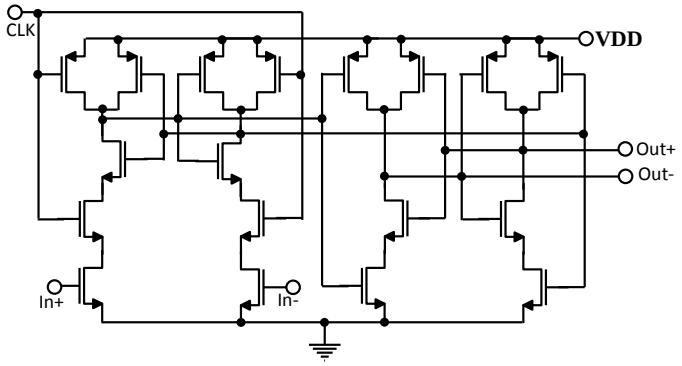

Fig. 5. Track and Latch comparator

IV. Simulation and Measurement Results

The system level simulation is performed in MATLAB to find out the key parameters and specifications of individual blocks. In simulation, the modulator has met all the specifications under strict trade-offs of noise and bandwidth (to accommodate up to EEG signal). The time domain response of the modulator in MATLAB is shown in Fig. 7, which shows the input sinusoidal waveform and modulated waveform. The frequency domain response of the modulator in MATLAB is shown in Fig.8. The simulated SNR is about 55.8dB. The transistor simulation has been done using Cadence SPECTRE and fabricated in a 0.18-µm CMOS technology. The total chip area is 2mm by 1.4mm including bond pad. The measured output plots are shown in Fig.9. and Fig.10 for sine wave input of 100Hz and 200Hz respectively. The measurement shows that the IC consumes around 20µA current at 1V power.

TABLE I. SUMMARY OF CHIP PERFORMANCE

Parameter	Simulated	Measured	Units
Supply Voltage	0.9 – 1.1	0.9 – 1.1	V
DC Current	17.58	20	µA
Input Frequency	100-500	100-500	Hz
SNR @ 200Hz	55.8	55	dB
SNR @ 500Hz	62	60	dB
OSR	32	32	
Input range	300-800	300-800	mV

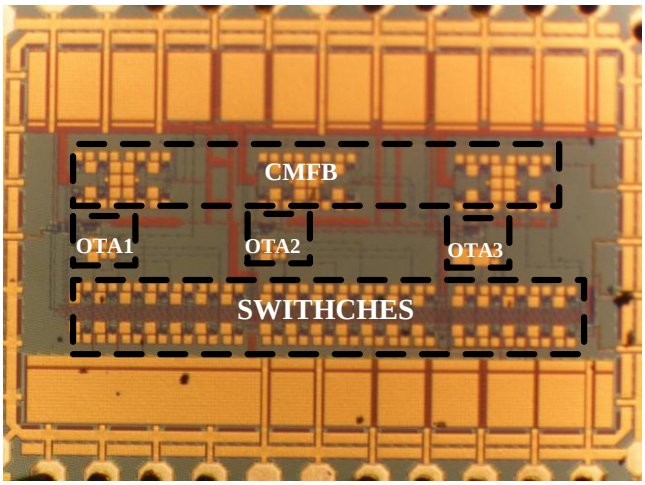

Fig. 6. Chip Micrograph

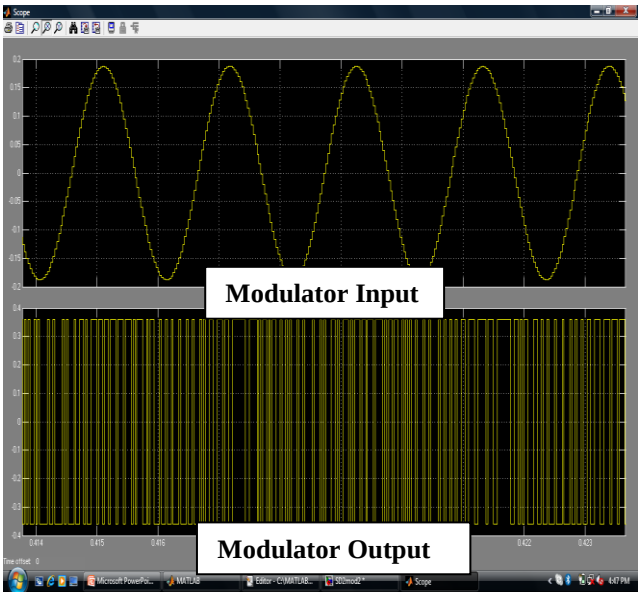

Fig. 7. Time domain Plot of Matlab system level simulation

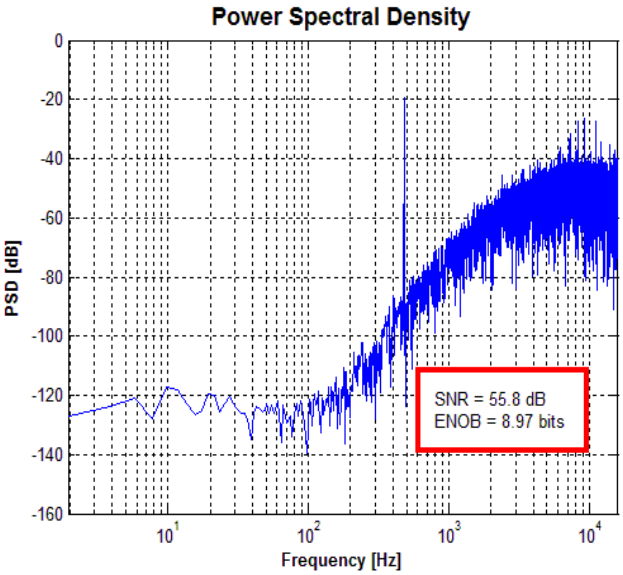

Fig. 8. Frequency domain Plot of Matlab system level simulation

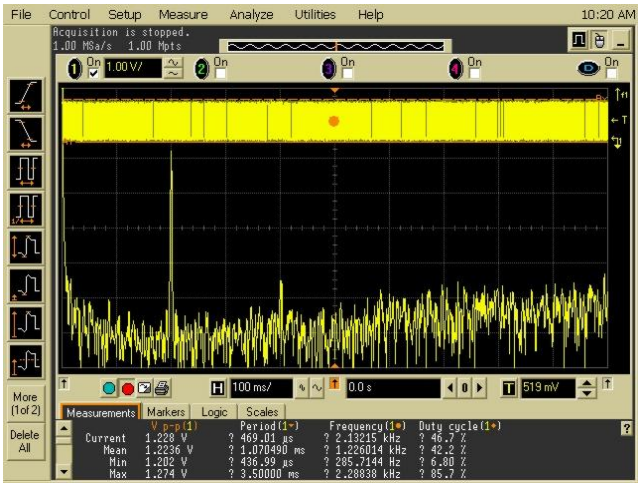

Fig. 10. Measured output spectrum with 200Hz input

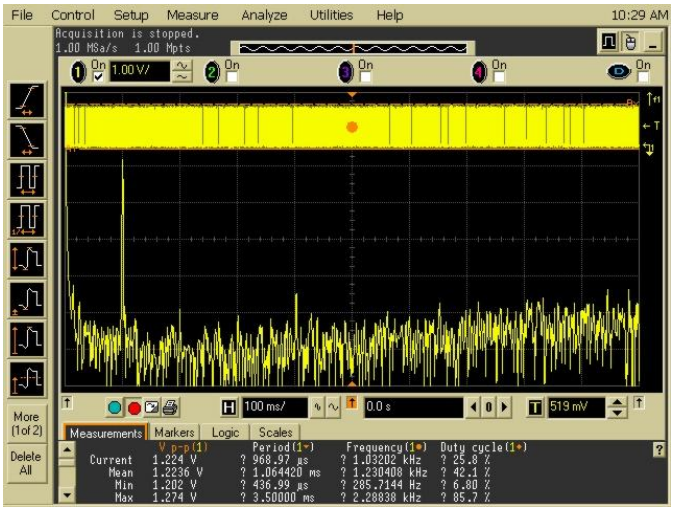

Fig.9. Measured output spectrum with 100Hz input

V.

ACKNOWLEDGMENT

The authors wish to acknowledge EHSII team members, and Integrated Circuits and Systems Laboratory staffs in IME for their invaluable inputs and comments.

VI.

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