High-speed String and Regular Expression Matching on FPGA

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Abstract—In recent FPGA researches, there has been much attention to dynamically reconfigurable algorithms that can modify their configuration on-the-fly. In this paper, we report recent progress on dynamically reconfigurable hardwares on FPGA for high-speed string and regular expression matching, which have been developed by our group since 2008. In particular, we describe the architecture, algorithms, and implementations of our pattern matching hardwares. We propose a pattern matching architecture, called dynamically reconfigurable bit-parallel NFA architecture which is the first dynamically reconfigurable hardware based on bit-parallel simulation of non-deterministic finite automata (NFA). This architecture enables fast dynamic reconfiguration of the patterns as well as high-throughput pattern matching for complex subclasses of regular expressions such as extended patterns, network expressions, and extended network expressions. In this approach, the information of an input NFA is compactly encoded in bit-masks stored in a collection of registers and block RAMs. Then, the NFA is efficiently simulated by a fixed circuitry using a combination of bit- and arithmetic-operations on these bit-masks consuming one input letter per clock. Experimental results show that our architecture has advantages over the previously proposed architectures in the terms of reconfiguration and running times.

I. INTRODUCTION

A. Backgrounds

By rapid growth of network and sensor technologies, mass storage of large amounts of data has emerged in various fields including networks and data engineering. ESP (event stream processing) [1] and NIDS (network intrusion detection system) [3] are example applications of data stream processing. Consequently, efficient data stream processing technologies have been extensively studied in theory and practice.

The large-scale pattern matching problem is one of the most important problems in data stream processing, where a pattern matching system has to work with a large number (e.g., thousands) of complex patterns (e.g., regular expressions) against high-speed data streams (e.g., several Gbps). These problems are, however, quite CPU-intensive tasks and it is difficult for software on a CPU to efficiently process massive data streams real-time in wire-speed. Therefore, researches on large-scale pattern matching on reconfigurable hardwares such as FPGA have attracted much attention recently ([3], [4], [5], [7], [10], [11], [13], [14]).

B. Our research goal

A recent research trend to large-scale regular expression matching hardwares is to simulate finite state automata for a given class of regular expressions on a specially designed hardware ([3], [4], [5], [10], [11], [13], [14]). Then, this approach is further classified into the static compilation approach and dynamic reconfiguration approach.

In the static compilation approach ([10], [11], [13], [14]), a set of input regular expressions is transformed into either deterministic finite automata (DFA) or non-deterministic finite automata (NFA) [9], and then statically compiled into wired logic on FPGA. However, the static compilation approach has a drawback that modification of regular expressions is too expensive to be done frequently.

In the dynamic reconfiguration approach ([3], [4], [5]), a universal control logic is statically compiled into FPGA beforehand, a description of regular expressions is loaded to the FPGA as data in the preprocessing phase, and then simulated in the run-time phase. This approach is attractive in real world applications such as EPS and NIDS where reconfiguration of input patterns frequently occurs. However, since classes of patterns that can be dealt with in this approach are still limited, our goal is to design dynamically reconfigurable hardwares that efficiently run for wider classes of regular expressions.

C. Main results

In this paper, we report recent progress on dynamically reconfigurable hardwares on FPGA for high-speed string and regular expression matching. We propose a novel pattern matching architecture, called dynamically reconfigurable bit-parallel NFA architecture. We show the top-level of our architecture in Fig. 1.

A pattern matching module (PMM, for short) is a core of our architecture, which is responsible for NFA-simulation of an input pattern. The key to the construction of a PMM is the use of bit-parallel NFA-simulation method developed in string matching communities since 1990 ([2], [9], [12]). In this method, the information of an NFA is compactly encoded...
in bit-masks. Then, the NFA is efficiently simulated by a fixed control logic using a combination of bit- and arithmetic-operations on these bit-masks consuming one input letter per clock [9].

An advantage of our architecture is the worst-case performance guaranteed by the design unlike the DFA-based architecture with micro controller [3]. Another advantage is the potential extensibility to more general pattern classes. For example, Kaneta et al. [6] recently extended the Extended SHIFT-AND method [9], used in this paper, to more general classes of network and regular expressions allowing union and the Kleene-star. Such method can be incorporated into our architecture by extending the construction of bit-masks and a circuitry described in this paper.

This paper is organized as follows. In Section II, we give basic definitions. In Section III, we propose our architecture, and in Section IV, we give the detailed description of a pattern matching module for extended patterns. In Section V, we give experimental results. In Section VI, we show an extension to more complex subclasses of regular expressions, and in Section VII, we conclude.

II. PRELIMINARY

A. Regular expression matching

Let \( N = \{0, 1, 2, \ldots \} \) be the set of all non-negative integers, and \( \Sigma = \{a, b, \ldots \} \) be a finite alphabet of letters. A string on \( \Sigma \) is a sequence \( S = s_1 \cdots s_n \) of letters, where \( S[i] = s_i \in \Sigma \) for every \( 1 \leq i \leq n \). We denote by \( S[i..j] \) the substring \( s_i \cdots s_j \) for every \( i \leq j \), and by \( \varepsilon \) the empty string. If \( i > j \), we define \( S[i..j] = \varepsilon \). For a set \( S \subseteq \Sigma^* \) of strings, we denote by \( |S| \) the cardinality and \( |S| = \sum_{s \in S}|s| \) the total size of \( S \). We denote by \( \Sigma^* \) the set of all strings on \( \Sigma \). For a letter \( a \in \Sigma \) and an integer \( i \in N \), we define by \( a^i \) the string consisting of \( i \) consecutive \( a \).

Let REG be the class of regular expressions on \( \Sigma \). More precisely, a regular expression \( R \) is either a letter \( a \in \Sigma \), concatenation \( R = R_1 \cdot R_2 \), union \( R = (R_1 | R_2) \), and the Kleene-star \( R = (R_1)^* \), where \( R_1 \) and \( R_2 \) are regular expressions [9]. For a regular expression \( R \in \text{REG} \), we denote by \( L(R) \subseteq \Sigma^* \) its language. Let \( T = t_1 \cdot \cdots \cdot t_n \in \Sigma^* \) be an input text of length \( n \geq 0 \), where \( t_i \in \Sigma \) (\( 1 \leq i \leq n \)). A pattern is a regular expression on \( \Sigma \). We say a regular expression \( R = r_1 \cdots r_m \in \text{REG} \) occurs at the end position \( j \) in \( T \), if \( T[i..j] = t_i \cdots t_j \in L(R) \). Our problem is stated as follows.

Definition 1. The multiple pattern matching problem for a subclass \( \mathcal{C} \subseteq \text{REG} \) of regular expressions is defined as follows. An input is an input pattern set \( \mathcal{P} = \{ (i, R_i) | i = 1, \ldots, N \} \subseteq \mathcal{C} \) (\( N \geq 1 \)), where for every \( i = 1, \ldots, N \), \( R_i \) is a pattern and \( i \) is an integer, called an index. Then, the task is, given a stream \( T = t_1 t_2 \cdots t_p \) (\( p \geq 1 \)) of input letters, to output the pairs \((i, p)\) such that \( i = 1, \ldots, N \) is the index and \( p \) is an end position of the \( R_i \) in \( T \) for all \( p = 1, 2, \ldots \).

B. Target pattern classes

The target subclasses of regular expressions that our architecture deals with are the classes of extended patterns (EXT), network expressions (NET), and extended network expressions (EXNET) defined as follows [9]. In what follows, \( \equiv \) means the notational equivalence.

An extended pattern (over \( \Sigma \)) in EXT is a regular expression in linear form, that is, \( R = r_1 \cdots r_m \) (\( m \geq 0 \)), where for every \( 1 \leq i \leq m \), \( r_i \) is one of the following forms: (i) letters \( a \in \Sigma \), (ii) wildcards \( . \in \Sigma \), (iii) classes of letters \( \alpha = [ab\ldots] \), (iv) optional letters \( \alpha ? \in (\alpha[\varepsilon]) \), (v) bounded repeats \( \alpha [x, y] \in (\alpha)^{y-x} \alpha^x \), and (vi) unbounded repeats \( \alpha * \in (\alpha\alpha) \), where \( \alpha \subseteq \Sigma \). Note that a letter \( a \in \Sigma \) and a wildcard \( \cdot \) are classes of letters. If a component \( r_i \) is one of the forms \( \alpha, \alpha [x, y], \alpha *, \) and \( \alpha + \), then \( \alpha \) is called the matrix of \( r_i \). We say that \( R \) is an exact string pattern (also called a string pattern), denoted by STR, if every component \( r_i \) of extended pattern \( R = r_1 \cdots r_m \) is a letter in \( \Sigma \).

A network expression (over strings) in NET is a regular expression without the Kleene-star, that is, a regular expression obtained from strings, concatenation, and union. An extended network expression in EXNET is a network expression over extended patterns.

Example 1. We show examples of string patterns (STR), extended patterns (EXT), network expressions (NET), and extended network expressions (EXNET):

- \( R_1 = ABABC \in \text{STR} \).
- \( R_2 = ([AB]+)(B\{1,3\})([BC]^?\cdot)^* \in \text{EXT} \).
- \( R_3 = A[ABB](B\{BA\}) \in \text{NET} \).

Fig. 1. The top-level of our pattern matching architecture.
• \( R_A = A(AB^+)(B^+)^* \), \( \{AB\}C \in \text{EXNET} \).

III. PROPOSED ARCHITECTURE

In this section, we present our dynamically reconfigurable bit-parallel NFA architecture based on bit-parallel NFA-simulation method ([2], [9], [12]). For the details, please consult our papers ([6], [7]).

In Fig. 1, we show the top-level of our pattern matching architecture on FPGA. Our architecture consists of an input decoder, a collection of pattern matching modules, and an output encoder. It receives and sends a sequence of I/O packets from and to a host PC through a fast bus such as PCI Express. In the present implementation, I/O packets have 64-bit length.

Our architecture runs with two different modes: the pre-processing mode and the run-time mode. In the pre-processing mode, our architecture loads the description of input patterns with packets and in the run-time mode, receives an input letter, makes a state transition for the target NFA by a fixed circuitry of a pattern matching module, detects matches, and emits a match information by receiving and sending packets.

IV. PATTERN MATCHING MODULE

A pattern matching module (PMM, for short) is a core of our architecture and efficiently simulates the NFA of an input pattern. The construction of a PMM depends on the class of an input pattern. In what follows, we give the construction of a PMM for the class EXT of extended patterns with fixed length \( L \) according to a bit-parallel method for EXT, called the Extended SHIFT-AND method [9]. In Fig. 2, we show the circuit of a pattern matching module for EXT.

Expanded form and bit-assignment. Let \( R \) be an extended pattern. Then, recall that every component \( r_i \) of \( R \) has one of the following types: (i) \( r_i = a \), (ii) \( r_i = a? \), (iii) \( r_i = a^+ \), (iv) \( r_i = a \{x, y\} \), where \( a \subseteq \Sigma \). Note that a letter \( a \in \Sigma \) and a wildcard ‘?’ are classes of letters of type (i). First, we expand all occurrences of bounded repeats \( a \{x, y\} \) of type (v) in \( R \) by using the equivalence \( a \{x, y\} \equiv \{a\}^{y-x} a^x \), where \( x \leq y \). Let \( \text{EXPAND}(R) = r_{1} \cdots r_{m} \) be the resulting expanded form of \( R \) consisting of \( m \) components, where \( |R| \leq m \leq L \). By the construction, the expanded form \( \text{EXPAND}(R) \) contains no occurrences of components of type (v). Then, we assign the unique numbers \( I = \{1, \ldots, m\} \), called the bit-positions, to all components of \( \text{EXPAND}(R) = r_{1}, \ldots, r_{m} \).

For example, let \( R_{2} = [AB]^+ B \{1, 3\}[BC]?^* \) be the target extended pattern consisting of six components. Then, by replacing the bounded gap \( \{1, 3\} \) with \( (?)\{?\}(?) \), we obtain its expanded form \( \text{EXPAND}(R_{2}) = ([AB]^+ B)(?)\{(?)\}(?)\{\} \) consisting of eight components with assigned bit-positions from 1 to 8.

Construction of DFA. Then, we obtain the extended pattern NFA \( N_{R} = N_{\text{EXT}}(R) \) for \( R \) from the expanded form \( \text{EXPAND}(R) \) as follows. Let \( \text{EXPAND}(R) = r_{1} \cdots r_{m} \) for some \( m \geq 1 \) and \( L \) be an positive integer larger than or equal to than \( m \). \( L \) is actually the bit-length of registers in an underlying hardware. By construction, we can assume that \( \text{EXPAND}(R) \) contains components of only type (i)–(iv). For every \( i = 1, \ldots, m \), we add to the NFA \( N_{R} \) edges related to state \( i \) according to the type of the \( i \)-th component \( r_{i} \) with matrix \( \alpha \) as follows:

- For all types (i)–(v) of \( r_{i} \), we add the backbone edge \( e_{i} = (i-1, \alpha, i) \) directed from the previous state \( i-1 \) to the current state \( i \) labeled with matrix \( \alpha \).
- Furthermore, if \( r_{i} \) is either (ii) \( \alpha? \) or (iii) \( \alpha^* \), then we add an \( \varepsilon \)-edge directed from the previous state \( i-1 \) to the current state \( i \).
- Furthermore, if \( r_{i} \) is either (iii) \( \alpha^* \) or (iv) \( \alpha^+ \), then we add a self-loop labeled with matrix \( \alpha \) from the current state \( i \) to itself.

For the expanded form \( \text{EXPAND}(R) = r_{1} \cdots r_{m} \), an \( \varepsilon \)-block in \( \text{EXPAND}(R) \) is the set \( B = \{i, i+1, \ldots, j\} \subseteq I \) of the component indexes for a maximal consecutive subsequence \( r_{i+1} \cdots r_{j} \) (\( 1 \leq i < j \leq m \)) connected with \( \varepsilon \)-edges, where \( r_{k} \) is either \( r_{k} = \alpha \gamma \) or \( r_{k} = \alpha \gamma^* \) for some \( i \leq k \leq j \). Let \( B_{1}, \ldots, B_{h} \) (\( h \geq 0 \)) be the \( \varepsilon \)-blocks of \( \text{EXPAND}(R) \). For
example, we show in Fig. 3 the extended pattern NFA $N(R_2)$ corresponding to $\text{EXPAND}(R_2)$. Then, $\text{EXPAND}(R_2)$ has two $\varepsilon$-blocks $B_1 = \{2, 3, 4\}$ and $B_2 = \{5, 6, 7\}$ corresponding to $r_3r_4 = (\cdot \cdot \cdot)$ and $r_6r_7 = (\cdot \cdot \cdot)(\cdot \cdot \cdot)$, respectively.

**Construction of bit-masks.** To simulate an extended pattern NFA $N$, we encode its information in the following five $L$-bit masks and two arrays of $L$-bit masks stored in a collection of registers and block RAMs, respectively:

- **INIT** is the $L$-bit mask that sets 1 at the bit-position for state 1. That is, $\text{INIT}[i] = 1$ if and only if $i = 1$.
- **ACCEPT** is the $L$-bit mask that sets 1 at the bit-position for the final state $m$. That is, $\text{ACCEPT}[i] = 1$ if and only if $i = m$.
- **EpsBEG** is the $L$-bit mask that sets 1 at the lowest bit-position of every $\varepsilon$-block. That is, $\text{EpsBEG}[i] = 1$ if and only if $i = \min(B_k)$ for some $\varepsilon$-block $B_k$.
- **EpsEND** is the $L$-bit mask that sets 1 at the highest bit-position of every $\varepsilon$-block. That is, $\text{EpsEND}[i] = 1$ if and only if $i = \max(B_k)$ for some $\varepsilon$-block $B_k$.
- **EpsBLK** is the $L$-bit mask that sets 1s at all bit-positions in every $\varepsilon$-block. That is, $\text{EpsBLK}[i] = 1$ if and only if $i$ is contained by some $\varepsilon$-block $B_k$.

**MOVE**[$\alpha$] is the $L$-bit mask that indicates all bit-positions of backbones labeled with a letter $\alpha \in \Sigma$ in $\text{EXPAND}(R)$. That is, $\text{MOVE}[\alpha][i] = 1$ if and only if $i$ is contained by some backbone labeled with $\alpha \in \Sigma$.

**REPPOS**[$\alpha$] is the $L$-bit mask that indicates all bit-positions of self-loops labeled with a letter $\alpha \in \Sigma$ in $\text{EXPAND}(R)$. That is, $\text{REPPOS}[\alpha][i] = 1$ if and only if the state $i$ has a self-loop labeled with $\alpha \varepsilon$, or equivalently, either $r_i = \alpha^*$ or $r_i = \alpha^+ \varepsilon$ with $\alpha \in \Sigma$.

In Fig. 4 and Fig. 5, we show examples of the bit-position assignment and the bit-masks for $R_2 = \text{EXPAND}(R_2)$ and its expanded form $\text{EXPAND}(R_2)$.

**Control logic for NFA-simulation.** We finally give the control logic for simulation of an extended pattern NFA $N$. Fig. 2 shows the whole circuit of NFA-simulation for EXT. This circuit is based on the codes of the Extended SHIFT-AND method [9].

First, the following code initializes the bit-mask $\text{STATE}$ that represents a set of active states at line (1) and applies the letter transitions by backbones and self-loops labeled with $t$ at lines (2) and (3), respectively, where $t \in \Sigma$ is the current input letter in an input text.

$$\text{STATE} \leftarrow ((\text{STATE} \ll 1) \mid \text{INIT})$$

$\& \text{ MOVE[\alpha]}$  \text{(2)}

$$\mid (\text{STATE} \& \text{REPPOS}[\alpha]);$$

Then, we simulate $\varepsilon$-transitions by the next codes. At line (4), we turn on the highest bit of each $\varepsilon$-block in $\text{STATE}$, and set it to HIGH. At line (5), for each $\varepsilon$-block in HIGH, we invert all bits lower than or equal to the lowest 1 bit of each $\varepsilon$-block in HIGH and set it to LOW. At line (6), the resulting bit-mask has 1s at all bit-positions properly higher than the lowest 1 of each $\varepsilon$-block in $\text{STATE}$. Finally, we add the change to $\text{STATE}$ at line (7).

$$\text{HIGH} \leftarrow \text{STATE} \mid \text{EpsBEG};$$

$$\text{LOW} \leftarrow \text{HIGH} \mid \text{EpsBEG};$$

$$\text{STATE} \leftarrow (\text{EpsBLK} \& (\sim \text{LOW}) \oplus \text{HIGH})$$

$$\mid \text{STATE};$$

The acceptance test is given by the following code.

$$\text{if} (\text{STATE} \& \text{ACCEPT}) \text{ then } \text{EmitMatch} \leftarrow 1;$$

In Fig. 6, we show an example of NFA-simulation by the set of bit-masks for $R_2 = \text{EXPAND}(R_2)$ and an input text $T = \text{ABCBBC}$. In the figure, we show the status of the bit-mask $\text{STATE}$ after the update in each cycle $i (1 \leq i \leq 6)$. The output $\text{EmitMatch}$ of a PMM is the value at the bit-position 8 of $\text{STATE}$.
TABLE I
Summary of parameters of the proposed pattern matching hardwares. See the text for the meanings of the parameter names.

<table>
<thead>
<tr>
<th>Class of Patterns</th>
<th>#Op</th>
<th>#Add</th>
<th>#Reg</th>
<th>#BL</th>
<th>#Slice</th>
<th>Freq (MHz)</th>
<th>Throughput (Gbps)</th>
<th>Load Time (μsec)</th>
<th>Total (#Patterns)</th>
<th>#Chars Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exact string patterns</td>
<td>5</td>
<td>0</td>
<td>3</td>
<td>250</td>
<td>54</td>
<td>363</td>
<td>2.9</td>
<td>0.182</td>
<td>256</td>
<td>8,192 letters</td>
</tr>
<tr>
<td>Extended patterns</td>
<td>12</td>
<td>1</td>
<td>6</td>
<td>512</td>
<td>123</td>
<td>202</td>
<td>1.6</td>
<td>0.328</td>
<td>128</td>
<td>4,096 letters</td>
</tr>
</tbody>
</table>

TABLE II
Results comparisons of regular expression matching hardwares based on various dynamically reconfigurable architectures, where Class indicates the target class, bRAM/char the number of bytes used in block RAMs per letter, and LC/char the number of logic cells used per letter.

<table>
<thead>
<tr>
<th>Design</th>
<th>Class</th>
<th>Device</th>
<th>Throughput (Gbps)</th>
<th>bRAM/char</th>
<th>LC/char</th>
<th>#Chars Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>KMP-based hardware [4]</td>
<td>STR</td>
<td>Virtex-2 Pro</td>
<td>1.8</td>
<td>4 bytes/char</td>
<td>3.2</td>
<td>3200</td>
</tr>
<tr>
<td>Bitsplit-based hardware [5]</td>
<td>STR</td>
<td>Virtex-4 FX100</td>
<td>1.6</td>
<td>46 bytes/char</td>
<td>1.4</td>
<td>16715</td>
</tr>
<tr>
<td>RegExp Controller hardware [3]</td>
<td>REG</td>
<td>Virtex-4 FX100</td>
<td>1.4</td>
<td>46 bytes/char</td>
<td>2.56</td>
<td>16715</td>
</tr>
</tbody>
</table>

V. EXPERIMENTAL RESULTS

To evaluate the time and area complexities, we implemented our pattern matching hardwares Dynamic BP-NFA in Verilog HDL for both classes STR and EXT of strings and extended patterns, where we set \( L = 32 \) and the arrays MOVE and REPP0S are implemented in block RAMs. Note that a PMM for STR has INIT, ACCEPT, and \( \langle MOVE(a) \rangle_{a \in \Sigma} \). For the details of a PMM for STR, see [7]. We targeted the Virtex-5 LX330 with -1 speed grade, which has 51,840 slices and 288 block RAMs with 36 Kbits. We used the Xilinx ISE Design Suite 10.1 and Synopsys VCS development tools. For comparison, we also implemented a hardware in the static compilation approach, called Static BP-NFA [8], based on the SHIFT-AND method [2] for STR on Xilinx Virtex-5 LX50 with 7,200 slices. For the details, see [8].

A. Results on our dynamically reconfigurable hardwares

In Table I, we show the summary of the experimental results of a single pattern matching module, PMM, in our dynamically reconfigurable hardwares Dynamic BP-NFA, where #Op, #Add, #Reg, #BL, and #Slice are the numbers of 32-bit operations, 32-bit integer additions, registers, block RAM lines per PMM, respectively. The number of block RAM lines (#BL) is given by the number of block RAMs times \( |\Sigma| = 256 \). #Patterns and #Chars Total are the number and the total size of input patterns, respectively. Below, we give results on our Dynamic BP-NFA and its comparisons against our previous static compilation hardware Static BP-NFA [8].

Performance evaluation. The maximum frequencies of our hardwares were 363 MHz and 202 MHz, respectively, for STR and EXT. For the time complexity in the run-time, we estimated the throughput of matching by Throughput = \( \text{Freq} \times 8 \) (bit/sec). Thus, the throughputs were 2.9 Gbps and 1.6 Gbps since our hardwares consume one letter (8 bits) per clock. On the other hand, the Static BP-NFA hardware achieved frequency of 216 MHz and throughput of 1.7 Gbps for 300 patterns in STR using 2,925 slices. Therefore, the dynamic version is faster than the static version.

Resource usage. For the Dynamic BP-NFA, we could implement up to 256 PMMs (8,192 total letters) and up to 128 PMMs (4,096 total letters), for STR and EXT, respectively. In this setting, the place-and-route took around one hour in both classes. For EXT, one PMM used 123 slices (total 15,744 slices) and two block RAMs (512 = 2×256 lines were used). Consequently, the usage of block RAMs was 89%, while the usage of slices was only 24%. This means that the size of a hardware in our architecture is constrained mainly by the amount of block RAMs and not by one of the slices. On the other hand, the Static BP-NFA used much less resources than the Dynamic BP-NFA. We could implement up to 1,500 PMMs (around 20K total letters) for STR using 7,200 slices (100%) and no block RAMs, where the slice usage seems linear in the number \( N \) of PMMs for \( N = 1 \) to 500 and seems almost constant for \( N = 500 \) to 1,500 ([8]).

Reconfiguration time comparison. We estimated the total loading time of a dynamically reconfigurable architecture by Load Time Total = #Patterns×(#Reg+#BL)/Freq (sec). From the result of Table I, the Dynamic BP-NFA took 0.71 μsec and 2.56 μsec per PMM to load an input pattern, and consequently, took the total loading times 0.182 msec and 0.328 msec to load all 256 and 128 patterns for STR and EXT, respectively. On the other hand, we estimated the loading time of the Static BP-NFA by the compilation time including place-and-route. By experiments, it required 4.27×10^5 msec for 300 PMMs, approximately seven minutes. Hence, the Dynamic BP-NFA is 10^6 times faster than the Static BP-NFA in load time.

B. Comparison against other pattern matching hardwares

In Table II, we compared our hardwares against the previous dynamically reconfigurable hardwares [3], [4], [5].

Performance evaluation. For the class STR, our hardware achieved higher throughput of 2.9 Gbps than Baker et al.’s KMP-based hardware [4] and Jung et al.’s Bitsplit-based hardware [5]. For more general classes of regular expressions, Baker et al.’s RegExp Controller hardware [3], which is a hybrid of DFA-simulation and microcontroller, has been the only dynamically reconfigurable architecture for a non-trivial
In this paper, we report recent progress on dynamically reconfigurable hardwares on FPGA for high-speed string and regular expression matching. For complex subclasses of regular expressions such as extended strings, network expressions, and extended network expressions, our architecture based on bit-parallel NFA-simulation method provides fast dynamic reconfiguration of the patterns as well as high-throughput pattern matching.

In experiment, we showed that our dynamically reconfigurable hardwares achieved throughputs of 2.9 Gbps and 1.6 Gbps for the classes of STR and EXT, respectively. In the present DPI (deep packet inspection) technology, where only the first several kilobytes of each packet is scanned, our hardwares’ throughputs look enough. However, further progress of DPI technology will require higher throughput. Therefore, it is a future research to make further speed-up of our hardwares.

In this paper, we considered end match information only. In recent applications such as ESP, however, it is also important to consider interval matches and non-overlapping matches. Therefore, it is an interesting problem to extend our hardwares to report matching information of both types.

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**REFERENCES**


**VI. EXTENSION TO NETWORK AND EXTENDED NETWORK EXPRESSIONS**

In Section IV, we gave the construction of a pattern matching module (PMM) for the class EXT of extended patterns based on the Extended SHIFT-AND method [9]. To extend the PMM for EXT to more complex classes, we developed a fast bit-parallel method, called the Extended² SHIFT-AND method, for the classes NET and EXNET of network and extended network expressions [6].
REFERENCES