A Low-Power Adaptive MIMO Detector for MIMO-OFDM WLAN Systems

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***Abstract*—A MIMO-OFDM receiver requests high-speed MIMO detection to separate spatially multiplexed signals on real-time processing, which causes large power dissipation due to its high throughput performance. We present an adaptive MIMO detector which adaptively changes the computational speed of MIMO detection by estimating Doppler shifts correlated with fading channel variations. The adaptive detector uses a DVFS technique which dynamically changes a clock frequency and a supply voltage according to the selected computational speed. This work discusses an 8x8 MIMO detector assuming single-user MIMO usage in IEEE802.11ac wireless LAN systems. The conventional and the proposed MIMO detectors have been evaluated in power dissipation.**

I. Introduction

Multiple-input multiple-output orthogonal frequency multiplexing (MIMO-OFDM) is powerful in enhancing communication capacity or reliance and is adopted in current wireless LAN standard of IEEE 802.11n [1]. IEEE 802.11ac, which is known as next standardization, supports eight spatial streams in single-user MIMO (SU-MIMO) [2]. As MIMO spatial streams increase, the computational and hardware complexities in MIMO-OFDM systems also greatly increase. It is a challenging to design a MIMO-OFDM transceiver with minimal hardware cost and power dissipation in VLSI implementation. Signal detection in a MIMO receiver, called MIMO detection, needs high-speed computation due to its large computational cost. Hardware implementation of MIMO detection is one important issue in current wireless communications. Algorithms for MIMO detection are linear detections [3], [4] ordered successive interference cancellation (OSIC) and non-linear detections [5], [6]. Maximum-likelihood (ML) detection [7], [8] is a non-linear detection. There are trade-offs between MIMO detection performance and computational complexity.

Recent researches have tackled linear detectors in minimum mean squared error (MMSE) for 4x4 MIMO-OFDM systems in terms of a trade-off between computational complexity and detector performance [9], [10]. Our presented MMSE MIMO detectors use pipeline processing on a subcarrier basis and are superior in throughput performance [11], [12]. However, they have not solve an issue in power increase for its high throughput performance. Our research group goes on LSI development of an 8x8 MIMO-OFDM transceiver compatible with the IEEE802.11ac specification. A low-power design is mandatory for further power increase of 8x8 MIMO. This paper describes the implementation of two 8x8 MIMO detectors

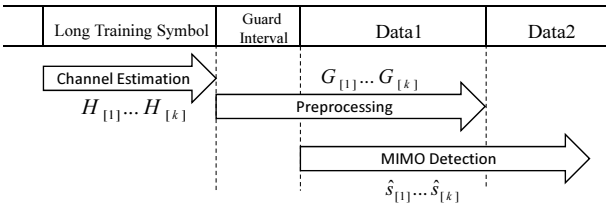


Fig. 1. Timing chart of a MIMO detection.

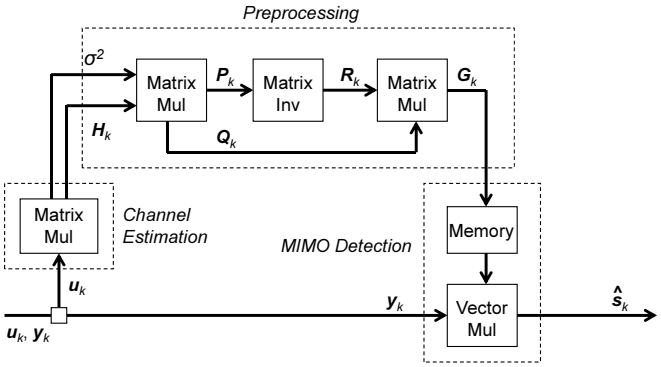


Fig. 2. Circuit structure of a MIMO detector.

and proposes an adaptive MIMO detector for power reduction. The proposed detector changes a clock frequency and a supply voltage in the detector according to a Doppler shift correlated with time variations in fading channels. The conventional and the proposed MIMO detectors have been evaluated in power dissipation.

II. Design of 8x8 MIMO Detectors

MIMO-OFDM received signals $\boldsymbol{y}[k,t]$ with M_T transmitter and M_R receiver antennas are described by

$$\boldsymbol{y}[k,t] = \boldsymbol{H}[k]\boldsymbol{s}[k,t] + \boldsymbol{n}[k,t], \tag{1}$$

where k is a subcarrier index, t is a data symbol index, $\boldsymbol{s}[k,t]$ is a signal transmitted at t-th symbol, and $\boldsymbol{n}$ is a white Gaussian noise vector. $\boldsymbol{H}[k]$ is a MIMO channel matrix whose elements are given the channel response from j-th transmitter antenna to i-th receiver antenna with k-th subcarrier. The linear MIMO detection is divided into zero-forcing (ZF) and MMSE.

The weight matrix $\boldsymbol{G}[k]$ in the MMSE criterion is given by

$$\boldsymbol{G}[k] = (\boldsymbol{H}_{[k]}{}^{H}\boldsymbol{H}_{[k]} + \sigma^2\boldsymbol{I})^{-1}\boldsymbol{H}_{[k]}{}^{H} \tag{2}$$

where $(\cdot)^H$ denotes the complex conjugate transpose, and σ^2 is the noise variance. The decoded signal $\hat{\boldsymbol{s}}[k,t]$ is given by multiplexing the weight matrix to the received signal.

$$\hat{\boldsymbol{s}}[k,t] = \boldsymbol{G}[k]\boldsymbol{y}[k,t] \tag{3}$$

The timing chart in Eqs. (2) to (3) is shown in Fig. 1, which consists of MIMO channel estimation, preprocessing (matrix inversion), and MIMO detection. The channel estimation extracts the MIMO channel matrix of $\boldsymbol{H}[k]$ from training symbols. The preprocessing calculates the inverted matrix of $\boldsymbol{G}[k]$. The MIMO detection decodes the original data from the received signals in the data symbols. When a MIMO-OFDM receiver computes the inverted matrix of $\boldsymbol{G}[k]$ and use it for the MIMO detection in the same packet, the preprocessing should finish by receiving the first data symbol.

The block diagram of a 8x8 MIMO detector is shown in Fig. 2. The input data in the MIMO detection block are given by the estimated MIMO channel matrix of $\boldsymbol{H}_k$ with k-th frequency bin and $M_T \times M_R$ matrix. The matrices of $\boldsymbol{P}_k$, $\boldsymbol{R}_k$, and $\boldsymbol{G}_k$ are computed as

$$\begin{aligned} \boldsymbol{P}_k &= \boldsymbol{H}_k^H\boldsymbol{H}_k + \sigma^2\boldsymbol{I} && (4)\\ \boldsymbol{Q}_k &= \boldsymbol{H}_k^H && (5)\\ \boldsymbol{R}_k &= \boldsymbol{P}_k^{-1} && (6)\\ \boldsymbol{G}_k &= \boldsymbol{R}_k\boldsymbol{Q}_k, && (7) \end{aligned}$$

The output data of $\boldsymbol{G}_k$ are stored in the memory unit and retrieved in the MIMO decoding process. We use Strassen's algorithm for the matrix inversion, which divides a square matrix into four block matrices. For an 8x8 matrix $\boldsymbol{\Omega}$, it is divided into 4x4 block matrices as

$$\boldsymbol{\Omega} = \begin{pmatrix} \boldsymbol{A} & \boldsymbol{B} \\ \boldsymbol{C} & \boldsymbol{D} \end{pmatrix}, \tag{8}$$

where $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}, \boldsymbol{D}$ are the 4x4 matrices. $\boldsymbol{\Omega^{-1}}$ is calculated by

$$\begin{aligned} \boldsymbol{\Omega}^{-1} &= \begin{pmatrix} \boldsymbol{F} & -\boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{E}^{-1} \\ -\boldsymbol{E}^{-1}\boldsymbol{C}\boldsymbol{A}^{-1} & \boldsymbol{E}^{-1} \end{pmatrix} \\ &= \begin{pmatrix} \boldsymbol{A}' & \boldsymbol{B}' \\ \boldsymbol{C}' & \boldsymbol{D}' \end{pmatrix}, && (9) \end{aligned}$$

$$\boldsymbol{F} = \boldsymbol{A}^{-1} + \boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{E}^{-1}\boldsymbol{C}\boldsymbol{A}^{-1} \tag{10}$$

$$\boldsymbol{E} = \boldsymbol{D} - \boldsymbol{C}\boldsymbol{A}^{-1}\boldsymbol{B}. \tag{11}$$

where $\boldsymbol{\Omega}$ is a Hermitian matrix composing $\boldsymbol{C} = \boldsymbol{B}^H, \boldsymbol{B}' = \boldsymbol{C}'^H$. This property gives the relation of $\boldsymbol{A}^{-1}\boldsymbol{B} = (\boldsymbol{C}\boldsymbol{A}^{-1})^H$. The calculation of $\boldsymbol{C}\boldsymbol{A}^{-1}$ can omit the calculation of $\boldsymbol{A}^{-1}\boldsymbol{B}$.

We have designed complete pipeline and 9-step pipeline MIMO detectors based on our previous works in [11], [12], whose architectures are depicted in Figs. 3 and 4, respectively. The complete pipeline connects all 4x4 matrix units of matrix adder, subtractor, multiplier, and inversion units. The matrix inversion unit computes the Strassen's matrix inversion in Eqs. (9)-(11). The delay units are inserted for adjusting pipeline latency delays. This architecture achieves the highest throughput performance by one data output per cycle, however needs considerable hardware. The 9-step pipeline divides the whole computation into 9 steps. The signal input of "Sel" in Fig. 4 is used for changing data paths in the matrix arithmetic units where different matrix operations are available in this dynamic reconfigurable architecture.

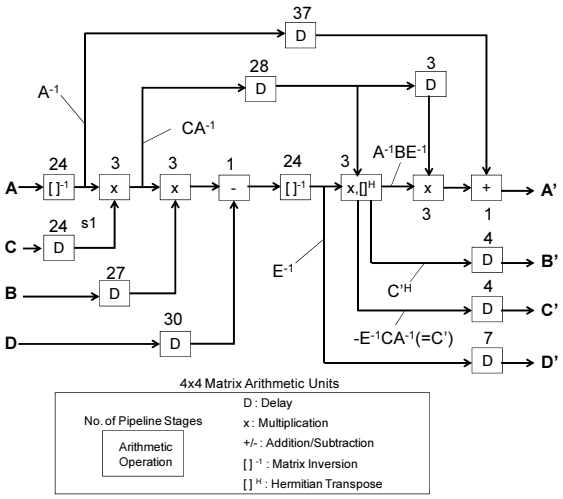


Fig. 3. Complete pipeline MIMO detector.

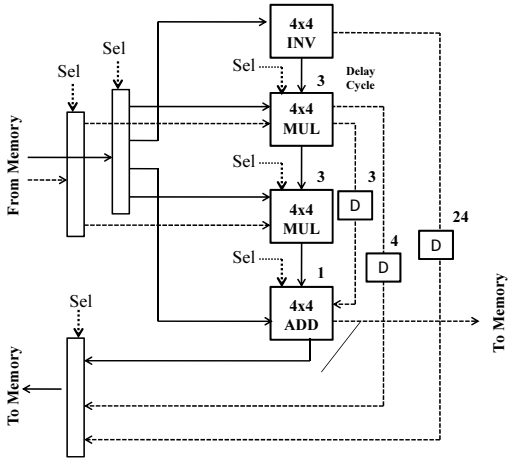


Fig. 4. 9-step pipeline MIMO detector.

The implementation results of 8x8 MIMO detectors on a 90-nm CMOS technology are shown in Table I, where a clock frequency was set to 100 MHz with 1.0-V supply voltage. The complete pipeline provides high-speed processing and increases a LSI scale. The circuit scale of the 9-step pipeline detector is smaller than that of the complete pipeline and has a longer processing delay.

TABLE I
IMPLEMENTATION RESULTS OF THE 8X8 MIMO DETECTORS.

	Complete Pipeline	9-Step Computation
Wordlength (bits)	26	24
Logic Gate Count	15.4 M	2.3 M
Clock Frequency (MHz)	100	100
Pipeline Latency (μs)	0.78	9.63
Power Dissipation (mW)	1,420	230

III. ADAPTIVE MIMO DETECTOR

A. Adaptive Detection

The high-speed MIMO detection is mandatory to follow time-varying fading channels in wireless LAN systems. However, if a mobile station does not move and stay on the same location for a long period, a speed of channel variation is quite slow. The graph in Fig. 5 shows time variations in MIMO channels for various Doppler frequency conditions. We use normailzed mean square error (NMSE) in this analysis. The simulation parameters in Table II are explained in Section IV. The NMSE value of $\xi(t)$ is computed as

$$\xi(t) = \frac{\sum_{k=1}^{K}\sum_{j=1}^{M_T}\sum_{i=1}^{M_R}|\hat{H}_{i,j,k} - H_{i,j,k}(t)|^2}{\sum_{k=1}^{K}\sum_{j=1}^{M_T}\sum_{i=1}^{M_R}|\hat{H}_{i,j,k}|^2} \quad (12)$$

where $\hat{H}_{i,j,k}$ is the channel matrix computed in the first packet with i-th column, j-th row, k-th subcarrier. $H_{i,j,k}(t)$ indicates the channel matrix computed in the other packets with a time interval of t. The variation of channel matrix depends on the parameters of Doppler frequency. This observation suggests that a receiver does not necessarily update a MIMO channel matrix for every packets for small Doppler frequency, which can extend the computation time in the MIMO detection.

The timing charts of MIMO detection methods are illustrated in Fig. 6. Figure 6(a) shows the conventional MIMO detection which computes and update the channel matrix for every packets. This method follows the time variation of high Doppler frequency condition. However, it requires high throughput in the MIMO detector and cause large power consumption. The adaptive MIMO detection shown in Figs. 6(b) and 6(c) skip the MIMO detection in some packets when a receiver detects low Doppler frequency. The case of the large detection delay is named as "method A", and the case of the small detection delay is named as "method B". Both methods skip 3 packets and update weight matrices for every 3 packets. The method A starts computing a weight matrix before 3 packets. Since this method has the detection delay by twice the number of skipped packets. On the other hand, the method B has the detection delay by only one packet. The method B has shorter computation time than the method A. However, the method B uses the newer information in the channel matrix than the method A and is superior in robustness with the channel variations.

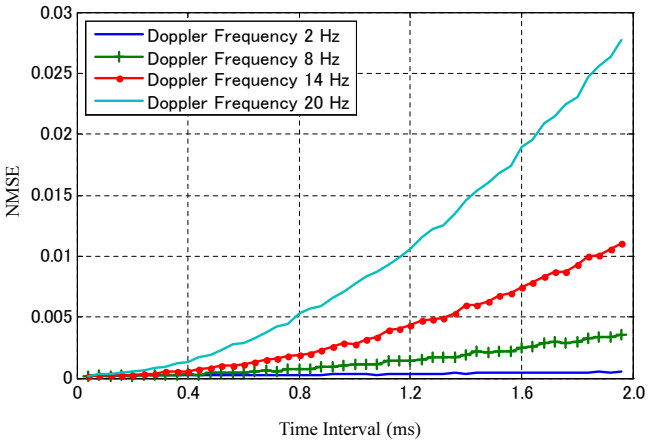
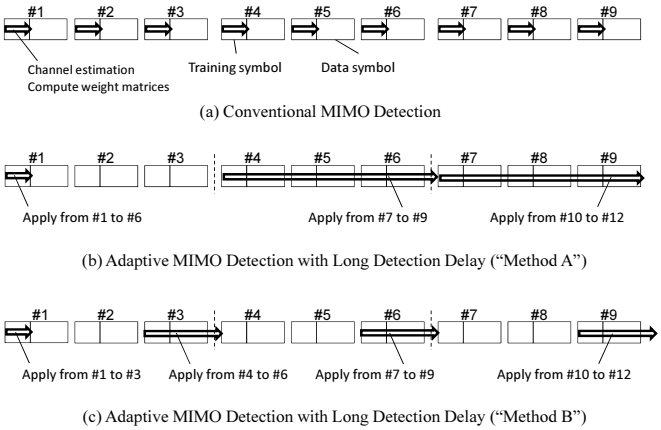


Fig. 5. Time variations in MIMO channels for Doppler frequency conditions.



(a) Conventional MIMO Detection

(b) Adaptive MIMO Detection with Long Detection Delay ("Method A")

(c) Adaptive MIMO Detection with Long Detection Delay ("Method B")

Fig. 6. Timing charts of MIMO detection methods.

B. DVFS Power Reduction

A DVFS technique [13] estimates and gives a dynamic operating voltage and frequency. When operating clock frequency is high, the high voltage is required. It causes large power consumption. When operating clock frequency is low, the voltage can be decreased. This case enables power reduction. The model of power consumption in CMOS circuits [14] can be expressed as

$$Power = C_L {V_{DD}}^2 f + (A-1) I_0 e^{\frac{-V_T}{\alpha V_{th}}} V_{DD}, \quad (13)$$

where C_L is a capacitance, V_{DD} is the operating voltage, f is the operating frequency, A is a number of gates, I_0 is a leakage current, V_T is a threshold voltage, V_{th} is a thermal voltage, and α is a factor of subthreshold parameters. The first term is a dynamic power which consumes during charging and discharging of additional capacity. The second term is a leakage power which consumes by a leakage current. From Eq. (13), a dynamic power is proportional to the square of the operating voltage, and a leakage power is proportional to

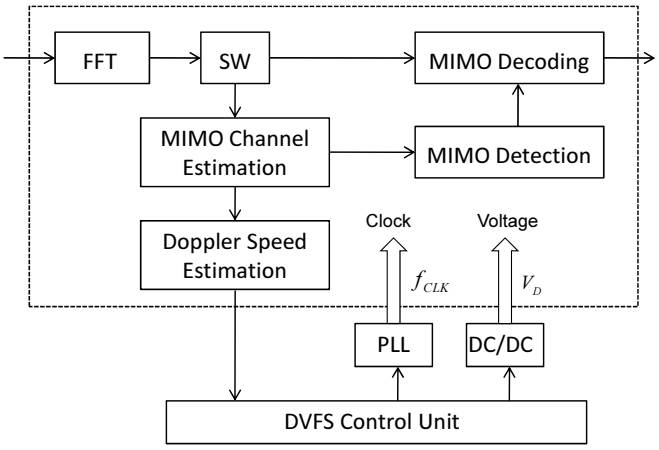


Fig. 7. Proposed adaptive MIMO detector.

TABLE II
SIMULATION PARAMETERS.

System	8x8 MIMO-OFDM
Modulation Type	16QAM
Signal Bandwith	40 MHz
FFT Size	128
No. of Data Subcarriers	108
FFT Length	3.2μs
Guard Interval Duration	0.8μs
Packet Length	500 Bytes
Channel Model	Multipath, Rayleigh Fading
MIMO Spatial Correlation	TGn Channel Model
Symbol Timing	Ideal
Doppler Frequency	2-20 Hz
Error Correcting	Convolution Coding (R=3/4) Soft-Decision Viterbi Decoding

the operating voltage. Power consumption of the whole circuit can be reduced in both a dynamic power and a leakage power by decreasing the operating voltage.

The adaptive MIMO detector with DVFS is shown in Fig. 7. The part under the dotted line operates in dynamic voltage and clock frequency estimated from the FFT outputs in received signals. A phase locked loop (PLL) and a DC/DC converter are used to change voltage and clock frequency dynamically. The DVFS control circuit estimates a Doppler frequency from the FFT outputs and gives the instruction of a clock frequency and voltage for the PLL and the DC/DC converter. Use of DVFS can deal with the change of the number of skipped packets when the Doppler frequency is changed.

IV. EVALUATION

A. Communication Performance

We decided the maximum numbers of skipped packets which do not cause performance degradation even in applying the adaptive MIMO detection. Bit error rate (BER) performance has been measured for the method A and the method B. The simulation parameters are enumerated in Table II. The simulation has been performed in Doppler frequency of 2 to 20 Hz. Figure 8 shows BER performance in the case of 10 Hz. The difference between the best and worst conditions for the

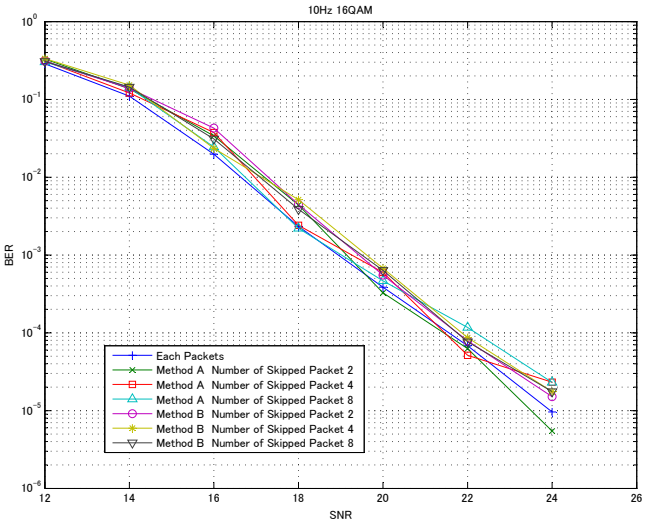


Fig. 8. BER performance in Doppler frequency of 10 Hz.

TABLE III
MAXIMUM NUMBERS OF SKIPPED PACKETS FOR DOPPLER FREQUENCY CONDITIONS.

Maximum number of skipped packets		Doppler frequency (Hz)				
		2	6	10	14	18
Method	A	4	4	4	2	2
	B	8	8	4	2	2

TABLE IV
EVALUATION RESULTS OF THE CONVENTIONAL AND THE PROPOSED MIMO DETECTORS.

Number of Skipped Packets	Computation Time (μs)	Clock Frequency (MHz)	Supply Voltage (V)	Power Dissipation (mW)
0 (w/o adaptation)	24	40	1.0	141.89
2	160	8	0.52	20.41
4	316	4	0.47	16.18
8	628	2	0.43	13.60

numbers of skipped packets is less than 1 dB in 24-dB SNR. It is decided as no performance degradation. Table III shows the simulation results in the maximum numbers of skipped packets for various conditions in Doppler frequency.

B. Power Consumption

The adaptive MIMO detection has been implemented into the pipeline 9-step MIMO detector explained in Section III. The evaluation results are shown in Table IV. The clock frequency has been determined by the estimated allowable processing time from the skipped packets in Table III. By lowering a clock frequency, a supply voltage can be decreased. The adaptive MIMO detector indicates maximum 90% of power reduction for the small Doppler frequency conditions.

V. CONCLUSION

We have presented an adaptive MIMO detector using DVFS to reduce power consumption in an 8x8 MIMO-

OFDM receiver. The adaptive MIMO detection skips packets performing MIMO detection. The DVFS decreases operating clock frequency and supply voltage. We have implemented the proposed detectors and evaluated power consumption. The proposed adaptive MIMO detector has reduced to 1/10 comparing with the conventional MIMO detector.

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REFERENCES

[1] "IEEE P802.11n/D4.00: draft amendment to wireless LAN media access control (MAC) and physical layer (PHY) specifications: enhancements for higher throughput," Mar. 2008.

[2] "Specification framework for TGac," doc.:IEEE 802.11-09/0992r21, Jan. 2011.

[3] V. Jungnickel, A. Forck, T. Haustein, et al., "1 Gbit/s MIMO-OFDM transmission experiments," IEEE Vehicular Technology Conference (VTC), Vol.2, pp. 25-28, Sep. 2005.

[4] Johan Eilert, DiWu, Dake Liu, "Efficient complex matrix inversion for MIMO software defined radio," IEEE International Symposium on Circuits and Systems (ISCAS), pp.2610-2613, May 2007.

[5] Zahid Khan, Tughrul Arslan, John S. Thompson, Ahmet T. Erdogan, "Area & power efficient VLSI architecture for computing pseudo inverse of channel matrix in a MIMO wireless system," the 19th International Conference on VLSI Design (VLSID), Jan. 2006.

[6] D. Perels, S. Haene, P. Luethi, A. Burg, N. Felber, W. Fichtner, H. Bolcskei, "ASIC implementation of a MIMO-OFDM transceiver for 192 Mbps WLANs," the 31st European Solid-State Circuits Conference (ESSCIRC), pp. 215-218, Sep. 2005.

[7] S. Chen, T. Zhang, M. Goel, "Relaxed tree search MIMO signal detection algorithm design and VLSI implementation," IEEE International Symposium on Circuits and Systems (ISCAS), pp.1147-1150, May 2006.

[8] Bjorn Mennenga, Emil Matus, Gerhard Fettweis, "Vectorization of the sphere detection algorithm," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2806-2809, May 2009.

[9] A. Burg, S. Haene, D. Perels, P. Luethi, N. Felber, W. Fichtner, "Algorithm and VLSI architecture for linear MMSE detection in MIMO-OFDM systems," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 4102-4105, May 2006.

[10] Hun Seok Kim, Weijun Zhu, Jatin Bhatia, Karim Mohammed, Anish Shah, Babak Daneshrad, "A practical, hardware friendly MMSE detector for MIMO-OFDM based systems," EURASIP Journal on Advances in Signal Processing, Vol. 2008, Article ID 267460, 14 pages, 2008.

[11] Shingo Yoshizawa, Yasushi Yamauchi, Yoshikazu Miyanaga, "VLSI implementation of a complete pipeline MMSE detector for a 4x4 MIMO-OFDM receiver," IEICE Transactions on Fundamentals, Vol. E91-A, No.7, pp. 1757-1762, July 2008.

[12] Shingo Yoshizawa, Hirokazu Ikeuchi, Yoshikazu Miyanaga, "VLSI implementation of a scalable pipeline MMSE MIMO detector for a 4x4 MIMO-OFDM receiver," IEICE Transactions on Fundamentals, Vol. E94-A, No.1, pp. 324-331, Jan. 2011.

[13] Ricardo Gonzalez, Benjamin. M. Gordon, Mark A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," IEEE Journal of Solid-State Circuits, Vol. 32, No. 8, pp. 1210-1216, Aug. 1997.

[14] D. Sengupta, R. Saleh, "Power-Delay Metrics Revisited for 90 nm CMOS Technology," IEEE International Symposium on Quality of Electronic Design (ISQED), pp. 291-296, March 2005.