A High Throughput MAC Layer for 600Mbps IEEE802.11n Wireless LAN

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***Abstract*—This correspondence presents a fast and systematic architecture for realizing an efficient 4-stream IEEE802.11n based hardware/software co-design Medium Access Control(MAC) Layer, which can achieve near theoretical MAC throughput for burst data transmission while complying with a strict channel access time requirements. As a design result, the proposed MAC system architecture can achieve 462Mbps for which 77% efficiency of maximum 4-stream Physical Layer(PHY) transmission rate 600Mbps is obtained. This result is verified with both SystemVerilog software simulation and hardware prototyping on a Xilinx FPGA board. Furthermore, a SoC architecture for one-chip implementation with MIPS/ARM/Power PC CPUs is also shown. In this SoC, IEEE802.11e as well as 11i functions are also included.**

I. Introduction

The Wireless Local Area Network (WLAN) is evolving rapidly, promising higher speed and better Quality-of-Serve (QoS) to enable fantastic multimedia applications and create new market opportunities.

IEEE802.11n standard promises high-throughput data rate up to 600Mbps at PHY Layer with a 4-stream MIMO elegant technique [1]. This high data rate has encouraged the widespread adoption of IEEE802.11 standards in today's wireless communication technology such as High Definition(HD) video streaming and Smart Phone usage over wireless networks. Nevertheless of increasing demands of huge number of packet transmission, the wireless channel has limited bandwidth. This limitatation results in higher packet error rates under such a huge packet transmission request situtation. In this aspect, QOS for WLAN system becomes more imprtant than ever.

The IEEE802.11e standard, which was estabiliehed in 2005, defines new QoS mechanism into 802.11in order to control access and usage of wireless medium based on different applications, providing tranffic differentiation and prioritization [2]. Specifically, a new burst access scheme know as Trasmission Opportunity(TXOP) with Block Acknowlegement(Block Ack) mechanism is introduced to satisfy the QoS for high bandwidth and low latency traffic.

The IEEE802.11n standard, on the other hand, defines MAC throughput above 450Mbps. Here, MAC throughput is defined as the total number of MAC Service Data Unit(MSDU) payload bits successfully transmitted divide by the total time taken to toransmit the MSDUs, which includes MAC channel access overheads and MAC architecture communication delay. In order to attain such high-throughput, the MAC layer needs to be designed by hardware and software co-design technique [3-5]. Table 1 shows both IEEE802.11n and 11e MAC Layer specification.

This paper introduces on the design and implementation of high-throughput MAC layer. In Sec. II, a new MAC architecture is prposed for dedicating hardware and software co-design technique. In Sec.III, we present some simulation results to verify the validity of the new MAC architecture by using System Verilog simulator for which both RTL and C-code are verified under virtual SoC verification environment. Sec. IV proposes a SoC architecture for one-chip design in terms of both MAC and PHY layer. Sec.V concludes the work.

TABLE I
MAC Specification

Standard	IEEE802.11n/11e
Network Topology	Base Service Set (BSS) for Infrastructure network(AP- STA)
Channel Access Protocol	Contention-based CA: DCF and EDCA
Supportable Frame Type	**Management:** Association Request/Response, Disassociation,Beacon, Authentication,Deauthentication **Control:** RTS, CTS, ACK, BA Req, BA, Control Wrapper, CF-End **Data:** Data, Null Data, QoS Data
Implemented Frame Exchange Sequence	1.Management+Broadcast(eg.Beacon) 2.(RTS CTS)Management+ ACK(eg.Association Request) 3.(RTS CTS) Data+group 4.(RTS CTS){Data+ACK} Data+ACK 5.(RTS CTS){Data+QoS} Data+QoS BlockAckReq BlockAck 6.(RTS CTS){Data+Qos+NoAck} Data+QoS+NoAck 7.(RTS CTS) {Data+QoS ACK} Data+QoS ACK 8.(RTS CTS){Data+QoS+HTC+AMPDU} Data+QoS+HTC+AMPDU BlockAck 9.{Data+QoS+HTC+AMPDU} Data+QoS+HTC+AMPDU BlockAckReq BlockAck

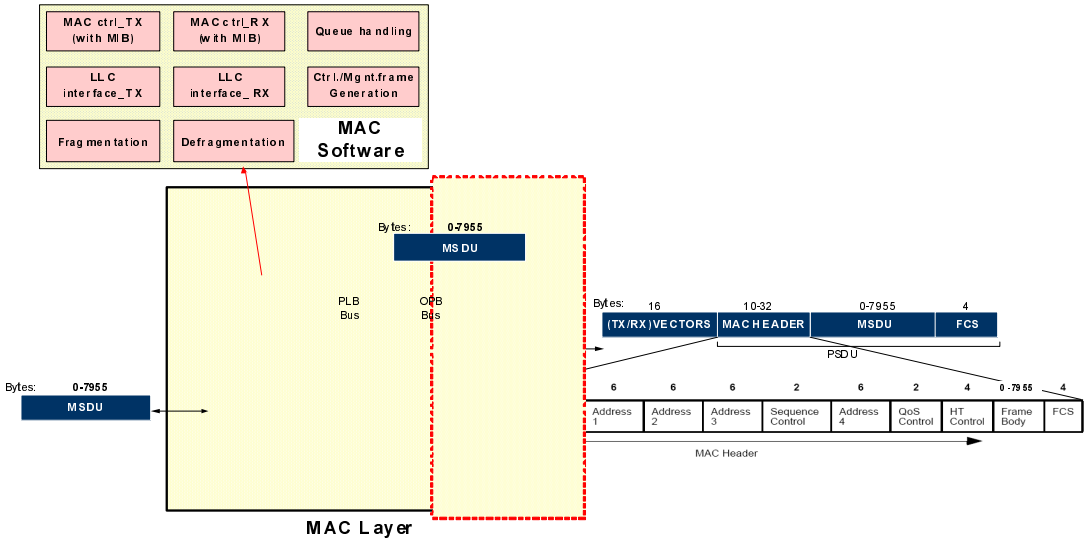

Fig. 2. MAC HW/SW Configuration

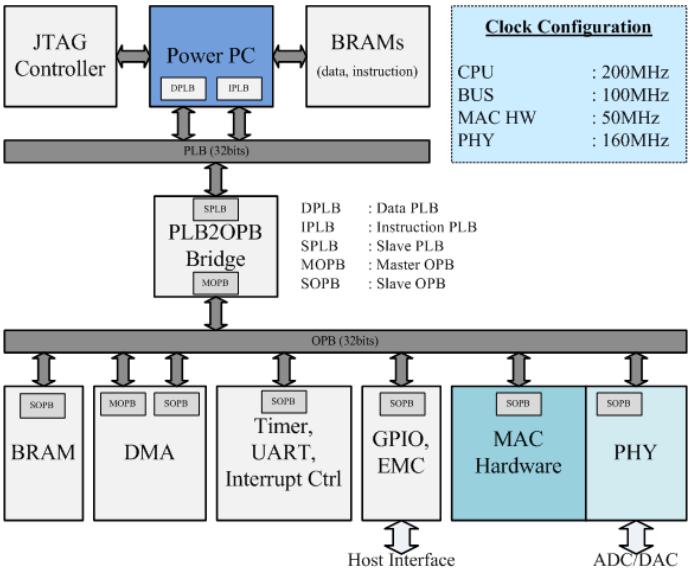

Fig. 1. PHY/MAC Architecture on PowerPC-based Verification Board

II. MAC Architecture

A. Prototype Architecture

Initially MAC system architecture has been designed using Xilinx embedded Reduced Instruction Set Computer (RISC) architecture PowerPC440. Fig.1 shows a MAC Architecture implemented on PowerPC-based Verification Board which is mounted with Xilinx FPGA (XC5VFX70T). The backbone of this architecture is the MAC hardware module attaches to the On-chip Peripheral Bus (OPB), and the MAC driver software program runs on the embedded PowerPC440 which attaches to Processor Local Bus (PLB). MAC hardware and software are interconnected through the PLB to OPB (PLB2OPB) bridge. Other Xilinx Intellectual Property (IP) cores, OPB interrupt controller, timer, General Purpose Input Output (GPIO) and External Memory Controller (EMC), have been used in this architecture.

B. Hardware Software Co-Design

Since target of this MAC system architecture is to achieve the high throughput which corresponds to IEEE802.11n standard PHY data rate of 600Mbps. To respond this requirement, the highly efficient hardware/software co-design MAC system has been considered. The MAC system is partitioned into hardware and software implementation based on the timing requirements for each MAC behavioral functions. Fig.2 shows the MAC HW/SW Configuration. About 28,000 4-inputs LUTs and 210 FIFO16/RAMB16 will be used for MAC hardware configuration, and 64kByte (Flash/SRAM) memory will be used for MAC software configuration.

C. Hardware Block Diagram

Fig.3 shows the block diagram of MAC hardware architecture. The data transmission process is as follows. Header Generation block generates MAC Protocol Data Unit (MPDU) delimiter for Aggregated-MPDU (A-MPDU) frame and MAC header for all frame types, and transmits MPDU data to Frame Check Sequence (FCS) Generation block. FCS Generation block appends FCS field before transferring the MPDU to next PLCP Transmit block which handles the interface protocol between MAC and PHY layers. For A-MPDU frame, aggregation function will be done in PLCP Transmit block.

Protocol Manager block signals PHY block to read TxVector and MPDU from PLCP Transmit block.

For data reception, PHY block transfers RxVector and MPDU from PLCP Receive block. Header Check block decodes and check the MAC header, while FCS Check block verifies FCS value. The Header Check blocks then interrupts MAC software to transfer the stored MSDU data to host user. Acknowledgement (ACK) Generation block generates ACK frame if it is necessary to transmit.

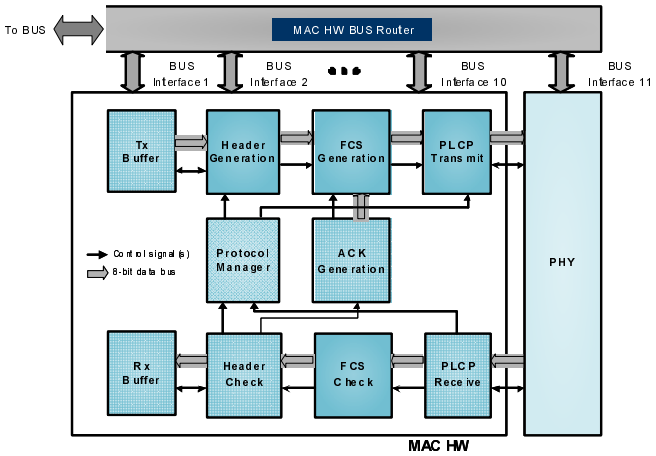

Fig. 3. HW Blockdiagram

III. Simulation

In this section, we demonstrate an efficiency of our developed MAC layer. IEEE802.11e standard defines efficient burst transmission of MPDU data frames with immediate Block Acknowledgement (BA). Fig.4. shows an aggregated MAC MPDU transmission with immediate BA for simulation purposes. Those MPDU comprises of burst data transmission while complying with a strict channel access time requirements. The next A-MPDU shall be prepared within 16us of Short Inter-Frame Space (SIFS).

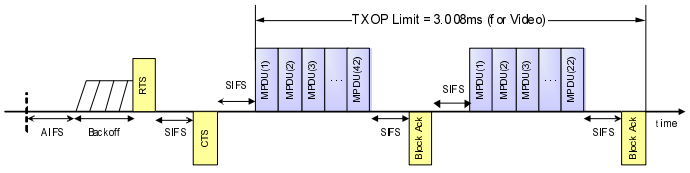

Fig. 4. Aggregation of MAC Protocol Date Unit (MPDU)

We have done the simulation for the throughput measurement with system verilog verification environment. Fig. 5. shows the simulation result of the throughput measurement of our MAC system. For this simulation, we set up CPU clock as 200MHz, OPB bus clock as 50MHz, MAC HW block clock as 50MHz and PHY data rate as 600Mbps. From this simulation result waveform, it can be seen that two A-MPDU packets, total 61 MPDUs, were transmitted within approximately 1584 us. Since each MPDU has a length of 1500Bytes, the calculated throughput becomes approximately 462Mbps. From this result, we can say that our MAC system can achieve the efficiency of more than 75% of PHY data rate.

IV. SoC Architecture

A SoC architecture with MIPS24 CPU for one-chip implementation in terms of both MAC and PHY layer is depicted in Fig.6. As an alternate of CPU, Power PC or ARM9 can be used and those CPU's C-code for MAC Layer also can be delivered. In addition, IEEE802.11e for QoS as well as 11i for encription functions are also included in this SoC. In addition, this IEEE802.11n chip supports protocol stack such as Ethernet so that it can be immediately used for market users' needs just in time without any development.

V. Conclusion

This paper has proposed a new MAC Layer architecture for IEEE802.11n WLAN sytem with hardware and software co-design methodology. Simulation results have shown that 462Mbps throughput can be obtained by using this MAC architecture. In addition, an SoC architecture implementing both MAC and PHY Layer has also been proposed. IEEE802.11e for QoS as well as 11i for encription functions are also included in this SoC. Furthermore, this IEEE802.11n chip supports protocol stack such as Ethernet so that it can be immediately used for market users' needs just in time without any development. We are now under back-end design of this SoC. Engineering samples will be delivered in 2012 2Q.

References

[1] IEEE Standard 802.11n TM 2009, Part11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications

[2] IEEE Standard 802.11e TM 2007, Part11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications

[3] Thet Htun Khine, Sangho Seo, Sung-Rok Yoon, Sin-Chong Park and Hiroshi Ochi, "IEEE802.11n Standard High Speed WLAN HT-MAC Development," No. B-05-138 Mar 2011.

[4] Min Li Huang, Jin Lee, Hendra Setiawan, Hiroshi Ochi and Sin-Chong Park, "A High Throughpur Medium Access Control Implementation Based on IEEE 802.11e Standard," IEICE Trans. Commun., vol.E93-B No.4 Apr 2010.

[5] Yuhei Nagao, Masayuki Kurosaki and Hiroshi Ochi, "Hardware Development of MIMO Wireless LAN using Model-Base Design,"*IEICE Trans*, No. AS-2-3,March 2010.

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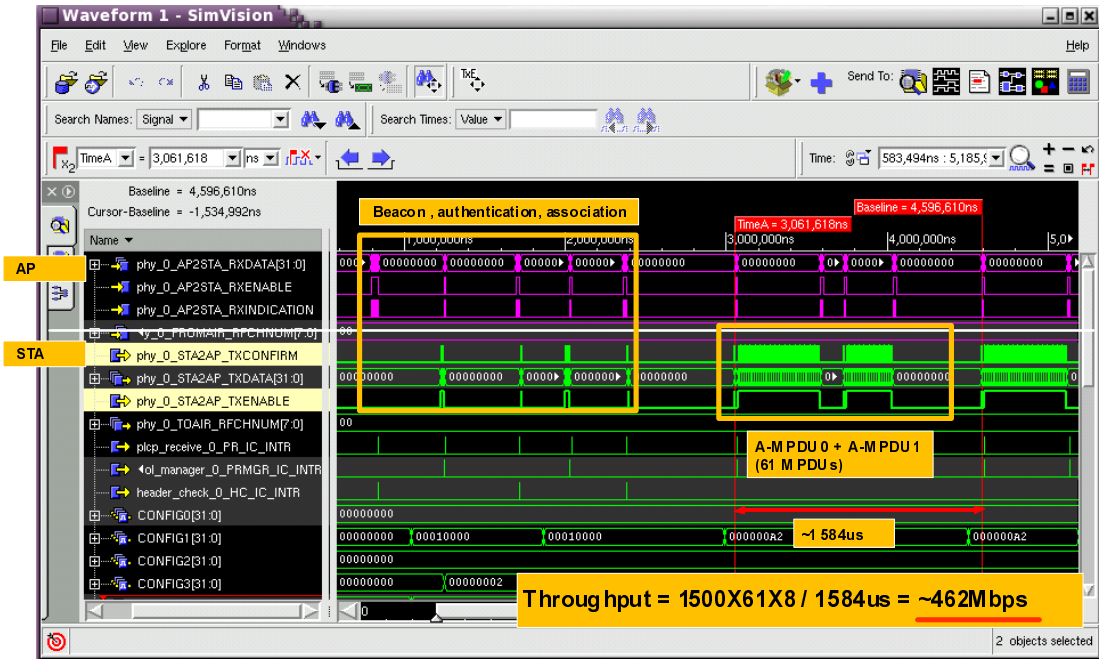

Fig. 5. System Verilog Verification for MAC Throughput Measurement

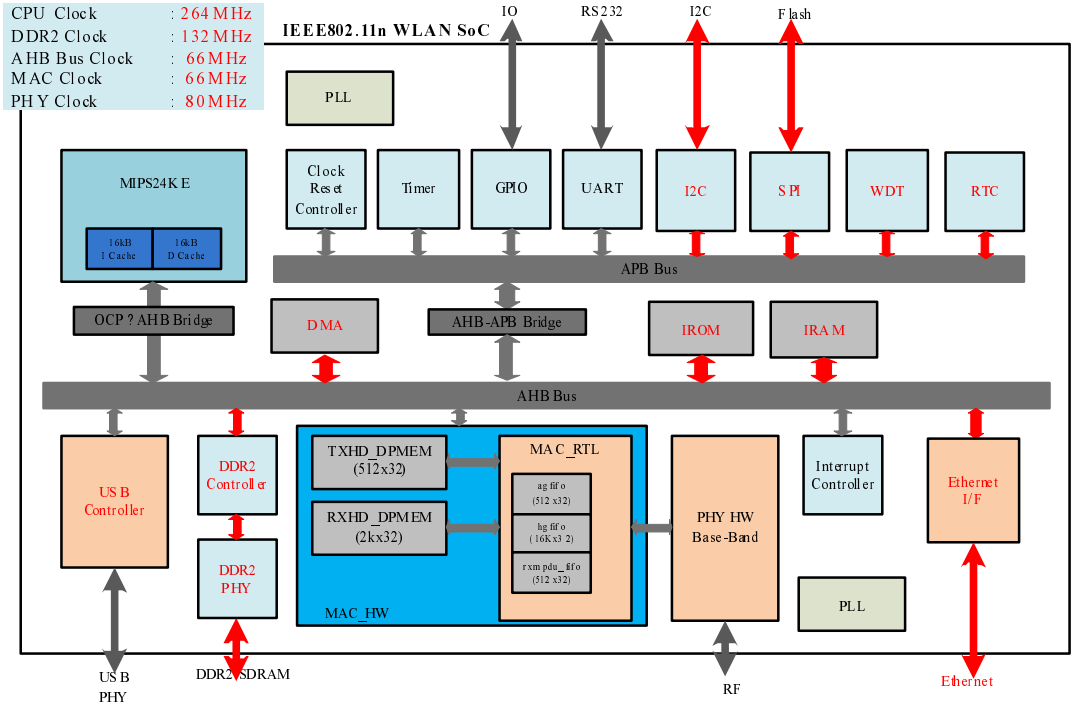

Fig. 6. 11n SoC Architecture with Peripherals