An Efficient VLSI Architecture of Parallel Bit Plane Encoder Based on CCSDS IDC

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***Abstract*— The Bit-Plane Encoder (BPE) is the key part of CCSDS-IDC that encodes the coefficients of 2-D Discrete Wavelet Transform (DWT). In common sense, it is considered as the bottleneck of throughput performance and hardware resource consumption. An efficient VLSI architecture of BPE implemented with parallel and pipeline technology is proposed in this paper. In this architecture, the whole bit planes of each DWT coefficient could be encoded simultaneously and pipeline is utilized in three functional parts of the bit plane coding. The proposed architecture has been implemented in a Xilinx FPGA, its throughput could be improved three times while its resource consumption is only about a quarter comparing with the published architectures.**

1. INTRODUCTION

With the rapid development of remote sensing technology, the image resolution is becoming higher and higher. Space missions are faced with the necessity of handling an extensive amount of imaging data. Image compression compensates for the limited on-board resources, in terms of mass memory and downlink bandwidth and thus provides a solution to the "bandwidth vs. data volume" dilemma of modern spacecraft [1]. In 2005, Consultative Committee for Space Data Systems (CCSDS) established a Recommended Standard for a data compression algorithm, namely CCSDS 122.0-B-1(Image Data Compression) standard [2].

The CCSDS IDC algorithm makes use of Discrete Wavelet Transform (DWT) to reach high compression ratio and high visual quality. There are also some other DWT-based image compression algorithm, for instance JPEG2000 [3], SPIHT [4] and No-List SPIHT algorithm. JPEG2000 has high compression performance but its high complexity makes it too difficult to implement in space application. SPIHT algorithm employs three lists to store significance information which consumes lots of memory. No-list SPIHT algorithm reduces the memory size but it has lower compression performance comparing with SPIHT [5].

The CCSDS IDC algorithm differs from image compression algorithm mentioned above in several respects: it specially targets high-rate instruments used on board of spacecraft and its low complexity supports fast and low-power hardware implementation [2]. Because of these advantages, CCSDS IDC algorithm is becoming more and more popular in space application. It consists of two functional parts, a DWT module that performs decorrelation and a Bit-Plane Encoder (BPE) which encodes the decorrelated data [2]. The Bit-Plane Encoder is the key part of CCSDS IDC and it is considered as the bottleneck of throughput performance and hardware resource consumption in common sense.

This paper presents an efficient VLSI architecture of BPE implemented with parallel and pipeline technology to overcome this bottleneck. Field Programmable Gate Array (FPGA) is a flight-proven hardware platform for high performance computing, as it has been used in a number of space missions [6]. The proposed architecture of BPE has been implemented in a Xilinx FPGA and its performance is improved greatly comparing with the published architectures.

The rest of this paper is organized as follows. In section 2, CCSDS IDC algorithm is introduced briefly. In section 3, the VLSI architecture and process flow are described and analyzed in detail. The experiment results and the performance are depicted in section 4. Finally, a conclusion is given in section 5.

2. ALGORITHM DESCRIPTION

The CCSDS IDC algorithm consists of two functional parts, depicted in Fig. 1, a Discrete Wavelet Transform module and a Bit-Plane Encoder. The DWT module makes use of a three-level two-dimensional Discrete Wavelet Transform with nine and seven taps for low-pass and high-pass filters to decorrelate image data and the Bit-Plane Encoder encodes the decorrelated data [2].

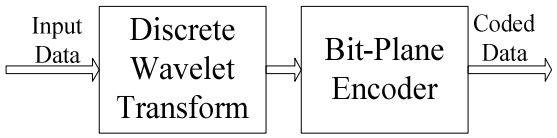

Fig.1 General Schematic of the Algorithm.

2.1 Discrete Wavelet Transform

There are two specific wavelets in CCSDS IDC standard: the 9/7 biorthogonal DWT, referred to as Float DWT, and a non-linear, integer approximation to this transform, referred to as Integer DWT. The Float DWT can obtain superior performance in the lossy domain, but only the Integer DWT supports strictly lossless compression. Fig. 2 illustrates a three-level two-dimensional DWT decomposition. Following this decomposition, ten subbands are generated and wavelet coefficients of these subbands are divided into 8×8 blocks. Each block is composed of a single coefficient from

subband LL_3, referred to as the DC coefficient, and 63 AC coefficients. An example of a block is revealed in Fig. 2 as comprised of shaded pixels [2].

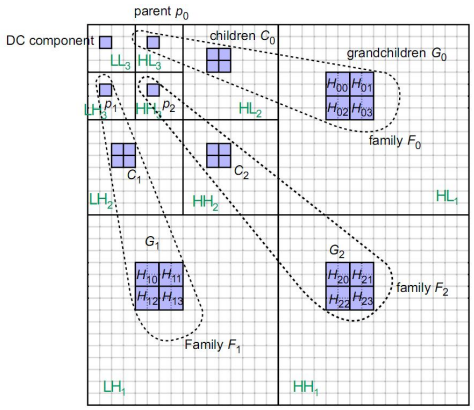

Fig. 2 Schematic of Wavelet-Transformed Image

2.2 Bit-Plane Encoder

The set of consecutive blocks are partitioned into groups called segments. The quantity of blocks can be assigned into any value between 16 and 2^{20} . The smaller the value is, the less resource is consumed and the more robustness is obtained, but the overall rate-distortion performance is poorer [7]. DWT Coefficients are encoded by the Bit-Plane Encoder segment by segment.

The Bit-Plane Encoder consists of DC coefficients encoder which performs initial coding of DC coefficients, referred to as DC encoder, and AC coefficients encoder that completes bit plane coding, referred to as AC encoder. The DC encoder computes BitDepthDC, BitDepthAC_Blockm and BitDepthAC [2] and then applies RICE algorithm to encode the quantized representation of the DC coefficients and BitDepthAC_Blockm.

The AC encoder processes the coefficients in three steps: it begins with coefficients significance scan and then encodes bit planes of significance information from most-significant bit plane to least-significant bit plane, finally it entropy encodes the words by using the variable-length binary codes. And the resulting encoded bit stream constitutes an embedded data format that provides progressive transmission within a segment [7].

3. VLSI ARCHITECTURE OF BPE

After DWT is applied, the DWT coefficients are encoded by BPE module. In the BPE module, DC encoder and AC encoder process the DWT coefficients simultaneously. These two encoders are independent of each other, so the parallel architecture is utilized to improve the hardware throughput performance. Fig. 3 illustrates the VLSI architecture of CCSDS IDC.

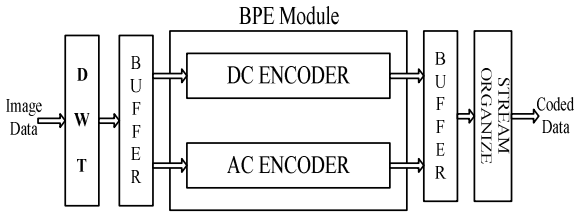

Fig.3 VLSI Architecture of CCSDS IDC.

3.1 DC encoder

The DC encoder applies RICE algorithm to encode the quantized representation of the DC coefficients and BitDepthAC_Blockm. The RICE algorithm consists of two functional parts: DPCM and entropy encoder. The entropy encoder exploits a set of variable-length codes to perform compression. Furthermore, an adaptive selection of code option is capable of achieving the highest compression. Finally, the coded bit stream is rearranged into bytes.

3.2 AC encoder

The AC encoder performs bit plane coding and it is the most complex part that constraints the throughput performance [5]. This paper proposes a novel parallel architecture utilizing pipeline technology partially to overcome the bottleneck of throughput and resource consumption.

The VLSI architecture of AC encoder is illustrated in Fig. 4. It consists of five functional parts: coefficients position map

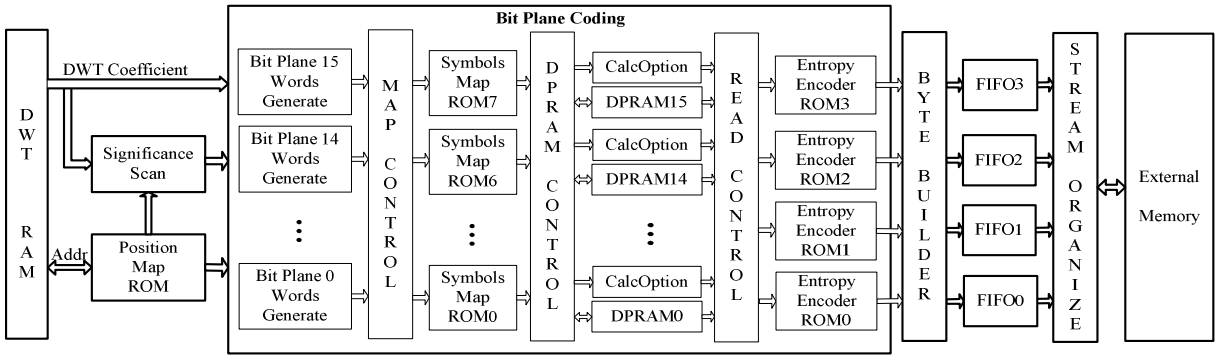

Fig.4 AC Encoder Architecture.

module, significance scan module, words generate module, symbols map module and entropy encoder module. Differing from the published parallel architecture [8, 9], the pipeline is used in significance scan module, symbols map module and entropy encoder module in this VLSI architecture. With parallel architecture, the whole bit planes of each DWT coefficient could be encoded simultaneously. Benefited from the pipeline architecture, the resource consumption is reduced greatly.

3.2.1 Coefficients Position Map Module

The AC coefficients with different data type (parent, children and grandchildren) are transformed into different binary words. Therefore the position information of AC coefficients should be supplied to bit plane coding module. A ROM stored the position information of a block is initialized in the position map module and coefficients of each block are sent to AC encoder one by one in the same order. All blocks are encoded by bit plane coding module consecutively and 64 clock periods are needed to process one block.

3.2.2 Significance Scan Module

The bit plane coding is performed in five stages: stage 0 is for DC refinement bits coding and the remaining stages (1-4) encode AC coefficients. The stage in which bits from AC coefficients in a bit plane are coded depends on the type of the AC coefficient at the bit plane [2]. This type value is similar to the significance defined in EZW [10], both of them are determined by the comparison result between coefficient value and threshold value.

A parallel significance scan method is used to improving coding efficiency in [9] but it consumes lots of hardware resources. In this paper, a novel bit plane significance scan scheme is designed. As shown in Fig. 4, the significance scan module is separated from the words generate module at each bit plane and the pipeline between significance scan and bit plane coding is employed.

In significance scan module, OR gates array is utilized in place of comparator to compute the significance and significance of all bit planes is reutilized by lower bit planes. Because of this architecture and the pipeline technology, the resource consumption of significance scan module is reduced greatly.

3.2.3 Words Generate Module

After the significance scan, the significance information of all bit planes is generated into some transition words simultaneously. The maximum DWT coefficient word size is determined by input image bit depth and DWT type [11]. Assumed the input is a 12-bit image, sixteen bit planes are necessary for bit plane coding. As illustrated in Fig. 4, sixteen words generate modules are implemented in the AC encoder.

At each bit plane, the coding is performed in five stages and all the transition words are generated in stage 1-3. There are 38 transition words in all and they are divided into 6 groups: tranB, tranD, tranG, tranHi, typesb[Ψ] and signsb[Ψ]. As Fig. 5 illustrated, different groups of words are generated concurrently but words in the same group can be generated by the same sub-module in pipeline. In this way, the resource consumption of words generate module is reduced to one sixth.

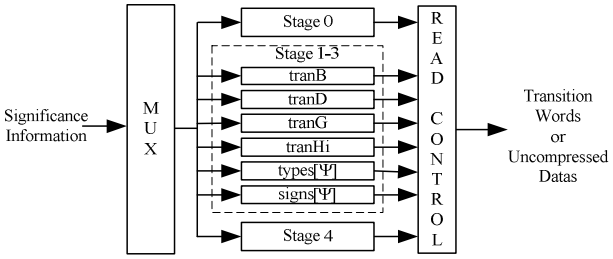

Fig. 5 Words Generate Module Architecture

3.2.4 Symbols Map Module

Before the entropy coding, transition words of length greater than one bit shall be mapped to integer values referred to as symbols. There are altogether 38 transition words but only 21 words at most need to be mapped to symbols. Because the sign bit words and words of one bit length are not coded further.

By the means of rearranging one sign bit word and one word need to be entropy coded into a long word, symbols map module processes one block in 21 clock periods. In this way, two bit planes can share one symbols map module and all the words are mapped to symbols in pipeline. Furthermore, the mapping table is stored in the ROM. Benefited from the pipeline and ROM, the resource consumption is decreased greatly. After the symbols mapping of a gaggle, the code option of entropy encoder is calculated by CalcOption module and the symbols are stored in dual port RAM at each bit plane.

3.2.5 Entropy Encoder Module

Entropy coding is adopted to improve the compression performance in CCSDS IDC. The symbols shall be encoded using variable-length binary words. Entropy coding is performed in the unit of gaggle, and in order to economize resource, pipeline technology is utilized again and the entropy encoder is implemented with ROM.

There are 16 bit planes but only 4 entropy encoders are sufficient to encode the symbols. Benefited from the combination of symbol and word, the time of reading dual port RAM is halved. Furthermore, once the type value of one coefficient is 1 at one bit plane, the bits of that coefficient at lower bit planes shall be processed in stage 4 and then some transition words may not exist at some bit planes.

In order to improve the entropy coding efficiency, all words and symbols in the dual port RAM shall be read out but only words and symbols with length greater than zero shall be written back into the RAM. In this way, all the valid symbols are stored in the RAM consecutively and the time for entropy encoding is decreased greatly. Therefore the pipeline could be

utilized in entropy encoder module and the pipeline structure is illustrated in Fig. 6. The entropy encoders encode the bit planes from most-significant bit plane to least-significant bit plane. Even though in the extreme situation, the higher bit planes is coded and included in the output bit stream.

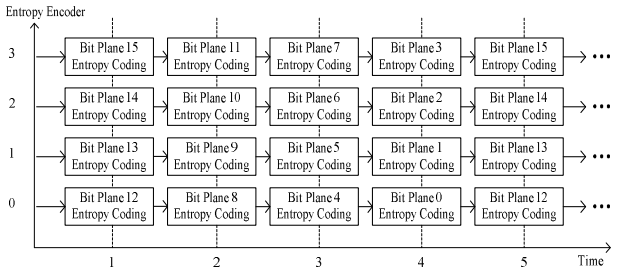

Fig. 6 Pipeline Structure of Entropy Coding

4. EXPERIMENTAL RESULTS

The proposed architecture is coded using Verilog HDL. The design has been implemented in the Xilinx VIRTEX Ⅱ XC2V3000-4BG728 FPGA using the Xilinx Integrated Software Environment (ISE) 10.1 version. The operation frequency of the proposed architecture can be up to 120.221 MHz. The detailed parameters of our FPGA implementation are listed in Table 1.

TABLE 1
FPGA IMPLEMENTATION RESULTS

Parameters	Used	Available	Utilization
Number of Slices	8172	14336	57%
Number of Slice Flip Flops	11288	28672	39%
Number of 4 input LUTs	13865	28672	48%
Number of BRAMS	56	96	58%
Frequency of operation	120.221 MHz		

The proposed architecture is compared with other similar designs and summary is given in Table 2. Architecture [5] utilizes the parallel block scan method which only achieves the throughput of 12.5 Msamples/s but consumes lots of hardware resource. Architecture [12] implements the CCSDS IDC in one DWT ASIC and one BPE ASIC, and this increases the complexity of the system though it can support the image of 16 bits. Architecture [13] has the throughput of 40 Msamples/s, however it has the highest resource consumption. Obviously the performance of the proposed architecture is much higher than the published architectures. With the parallel bit plane coding scheme and pipeline technology, the proposed architecture's throughput is improved three times while its resource consumption is only about a quarter comparing with the published architectures.

TABLE 2
COMPARISON WITH OTHER DESIGNS

Architecture	Bits Per Pixel	Throughput	Slices	Technology
[5]	---	12.5 Msps	23036	XC2V6000 -4
[12]	16	20 Msps	---	ASIC
[13]	12	40 Msps	29648	XQR5VFX130 -1
Proposed	12	120 Msps	8172	XC2V3000 -4

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5. CONCLUSION

In this paper, an efficient VLSI architecture of bit plane encoder based on CCSDS IDC is presented. This architecture's throughput performance is up to 120 Msamples/s with the parallel bit plane coding method. In order to reduce the resource consumption of parallel architecture, pipeline technology is utilized in three functional parts of the bit plane coding module. By these means, lots of hardware resource is economized and the architecture is implemented in the Xilinx VIRTEX Ⅱ XC2V3000-4BG728 FPGA.

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