Invited Overview Session

Session: FP1-1.2
Time: Friday, December 18, 14:30 - 15:00
Place: Room Y301
Chair: Daniel P.K. Lun, The Hong Kong Polytechnic University (Hong Kong)

From Algorithm/Architecture Co-Exploration to Internet of Things

Speaker: Gwo Giun (Chris) Lee, National Cheng Kung University, Taiwan

Abstract
NIKLAUS EMIL WIRTH introduced the innovative idea that Programming = Algorithm + Data Structure. Inspired by this, the current talk advances the idea to the next level by stating that Design = Algorithm + Architecture. With concurrent exploration of both algorithm and architecture entitled Algorithm/Architecture Co-exploration (AAC), this methodology introduces a leading paradigm shift in advanced system design including cloud computing and Internet of Things.

As computing becomes exceedingly demanding and data becomes increasingly bigger, efficient parallel and flexible reconfigurable processing are crucial in the design of signal processing systems. Hence the analysis of algorithms for potential computing in parallel is crucial. AAC presents a technique which systematically lays out the full spectrum of potential parallel processing components eigen-decomposed into possible data granularities. With data dependency minimization, this spectrum of independent graph components is resolved from a particular data granularity into lower and mixed granularities within the design space. This makes possible the study of potentials for homogeneous or heterogeneous parallelization at different granularities as opposed to conventional systolic array for homogeneous designs at single fixed granularity with possible extensions to distributed computing on cloud platforms. Because AAC was targeted for SoC systems with versatile platforms, the scope of system is extensible to systems connected via signals in conveying information thus forming Internet of Things (IoT). This introduces a fundamental framework for general system design already with major impact to SoC systems and has been broaden to cloud computing, Deep Learning in machine learning, and even genomic and proteomic signal processing systems in bioinformatics.

Biography

Gwo Giun (Chris) Lee (S'91-M'97-SM'07) received his B.S. degreein Electrical Engineering from National Taiwan University and both his M.S. and Ph.D. degrees in Electrical Engineering from University of Massachusetts. Dr. Lee has held several technical and managerial positions in the industry including System Architect in former Philips Semiconductors, USA, DSP Architect in Micrel Semiconductors, USA, and Director of Quanta Research Institute, Taiwan before joining the faculty team of the Department of Electrical Engineering in National Cheng Kung University (NCKU) in Tainan, Taiwan where he established the Media SoC Laboratory. He was also a

visiting Professor at "Swiss Federal Institute of Technology" (EPFL), Switzerland during 2007. Dr. Lee has authored more than 200 technical papers and is currently a member of the ISO/IEC MPEG standardization committee and was also the chief editor for the Reconfigurable Video Coding (RVC) Ad Hoc group. He was the Chair for the Complexity Analysis Ad HoC Group of ISO/ IEC ITU JVT-3V in 3D Video Coding. Dr. Lee also serves as the Associate Editor for both IEEE Transactions on Circuits and Systems for Video Technology from 2009 till 2013 and Journal of Signal Processing Systems since 2010.

He received the Best Associate Editor's Award for IEEE Transactions on Circuits and Systems for Video Technology in 2010 and the Best Paper Award for the BioCAS track in ISCAS 2012. Dr. Lee was also the Guest Editor for IEEE TCSVT's November, 2009 special issue on "Algorithm/ Architecture Co-Exploration for Visual Computing on Emergent Platforms". He is the Chair of the technical committee for "Visual Signal Processing & Communications" track and member of "Multimedia Systems Application" track for IEEE International Symposium on Circuits and Systems (ISCAS). Dr. Lee also serves as the technical committee member for both the Digital Implementation of Signal Processing Systems (DISPS) and the Industry Digital Signal Processing (IDSP) committees for IEEE Signal Processing Society and Circuits and Systems Society. Furthermore, he is currently the Chair of the Signal Processing Systems Track in Asia Pacific Signal and Information Processing Association (APSIPA). His research interests are focused on intelligent and biomedical algorithm, architecture, VLSI/SoC design, and Algorithm/Architecture Co-Exploration (AAC) for signal and information processing systems including cloud computing and Internet-of-Things.